PHIL-05955

Colour Television **Module**

Service
Service
Service

SDI PDP Repair Manual

S37SD-YD02 (37-inch SD v4)
S42SD-YD05, YD06, YD07 (42-inch SD v2, v3, v4)
S42AX-XD02, YD01 (42-inch HD v3, v4)
S50HW-XD03, XD04 (50-inch HD v3, v4)

ServiceManual

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1. Technical Specifications, Connections, and Chassis Overview

Index of this chapter:
1.1 PDP Overview
1.2 Serial Numbers
1.3 Chassis Overview

Notes:
- Figures can deviate due to the different model executions.
- Specifications are indicative (subject to change).

1.1 PDP Overview

Table 1-1 PDP overview

	PDP Type/Version	Model Name	H x V Pixel
1	37" SD v4	S37SD-YD02	852 x 480
2	42" SD v2	S42SD-YD06	852 x 480
3	42" SD v3	S42SD-YD05	852 x 480
4	42" SD v4	S42SD-YD07	852 x 480
5	42" HD v3	S42AX-XD02	1024 x 768
6	42" HD v4	S42AX-YD01	1024 x 768
7	50" HD v3	S50HW-XD03	1366 x 768
8	50" HD v4	S50HW-XD04	1366 x 768

Table 1-2 PDP vs Chassis overview

Display type	Model #	Chassis	Chassis Manual #
37" SD v4	37PF9936/37	LC4.7U	3122 785 14742
37" SD v4	37PF9946/12	LC4.7E	3122 785 14722
37" SD v4	37PF9946/69	LC4.7A	3122 785 14761
42" SD v2	420P20/00	FM242	3122 785 14130
42" SD v2	42FD9925/01	FM242	3122 785 14130
42" SD v2	42FD9935/17	FM242	3122 785 14130
42" SD v2	42FD9935/93S	FM242	3122 785 14130
42" SD v2	42FD9945/01	FM242	3122 785 14130
42" SD v2	42FD9953/17, /69, /93	FM242	3122 785 14130
42" SD v2	42HF9953/12Z	FM24_AB	3122 785 13890
42" SD v2	42PF9936/37	FTP1.1U	3122 785 14381
42" SD v2	42PF9945/12	FTP1.1E	3122 785 14370
42" SD v2	42PF9945/69, /79, /98	FTP1.1U	3122 785 14381
42" SD v2	42PF9955/12	F21RE	3122 785 13890
42" SD v3	42PF9936D/37	LC4.7U	3122 785 14742
42" SD v3	42PF9946/12	LC4.7E	3122 785 14722
42" SD v3	42PF9946/79, /93, /98	LC4.7A	3122 785 14761
42" SD v3	42PF9956/12	FTP2.2E	3122 785 14651
42" SD v3	42PF9956/93	FTP2.2A	3122 785 14680
42" SD v4	42PF7320/10	LC4.9E	3122 785 15431
42" SD v4	42PF7320/79, /98	LC4.9A	3122 785 15450
42" HD v3	42PF9966/37	FTP2.2U	3122 785 14662
42" HD v3	42PF9966/79, /93, /98	FTP2.2A	3122 785 14680
42" HD v3	42PF9976/37	FTP2.2U	3122 785 14662
42" HD v4	42HF7543/37	BP2.3HU	3122 785 15900
42" HD v4	42PF7320A/37	BP2.3U	3122 785 15541
42" HD v4	42PF7520D/10	LC4.9E_AB	3122 785 15670
42" HD v4	42PF9630/78	FTP2.4L	3122 785 15470
42" HD v4	42PF9630A/37	BP2.2U	3122 785 15541
42" HD v4	42PF9630A/96	BP2.2U	3122 785 15541
42" HD v4	42PF9966/79, /98	FTP2.4A	3122 785 15470
50" HD v3	50PF9956/37	FTP2.2U	3122 785 14662
50" HD v3	50PF9966/12	FTP2.2E	3122 785 14651
50" HD v3	50PF9966/37	FTP2.2U	3122 785 14662
50" HD v3	50PF9966/69, /93	FTP2.2A	3122 785 14680
50" HD v4	50HF7543/37	BP2.3HU	3122 785 15900
50" HD v4	50PF7320/10	LC4.9E	3122 785 15431
50" HD v4	50PF7320/79, /93, /98	LC4.9A	3122 785 15450
50" HD v4	50PF9630/78	LC4.9L	3122 785 15450
50" HD v4	50PF9630A/96	BP2.2U	3122 785 15541
50" HD v4	50PF9830A/37	BP2.1U	3122 785 15541
50" HD v4	50PF9966/79	FTP2.4A	3122 785 15470
50" HD v4	50PF9967D/10	FTP2.4E_AB	3122 785 15740

In above table the link is given between the SDI Plasma Display Panel and the Philips TV chassis (incl. chassis manual no.).

1.1.1 37" SD v4

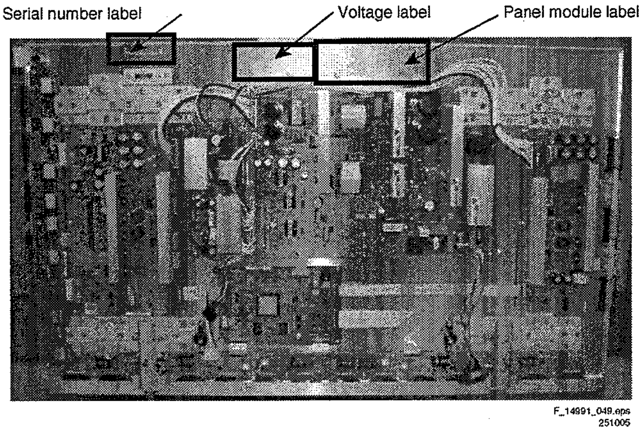

Figure 1-1 External view (37" SD v4)

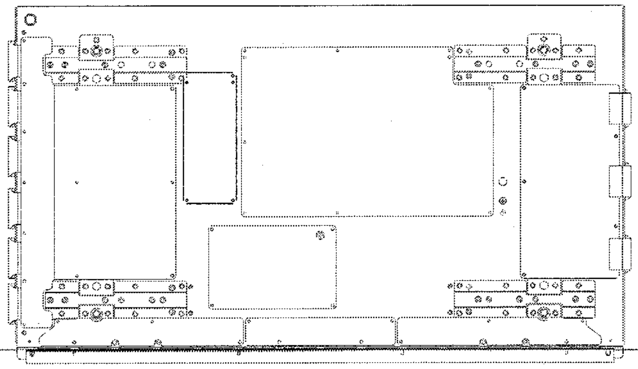

Figure 1-2 Points of screw mount (37" SD v4)

No	Item	Specification 37" SD v4	
1	Pixel	852 (H) x 480 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	2556 (H) x 480 (V)	
3	Pixel Pitch	0.960 mm (H) x 0.960 mm (V)	
4	Cell Pitch	R	0.320 (H) mm 0.960 (V) mm
		G	0.320 (H) mm 0.960 (V) mm
		B	0.320 (H) mm 0.960 (V) mm
5	Display size	817.92 (H) x 460.80 mm (V)	
6	Screen size	Diagonal 37" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 52.9 (D) mm	
11	Weight	Module 1	About 15.5 kg
12	Broadc. reception Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.2 42" SD v2

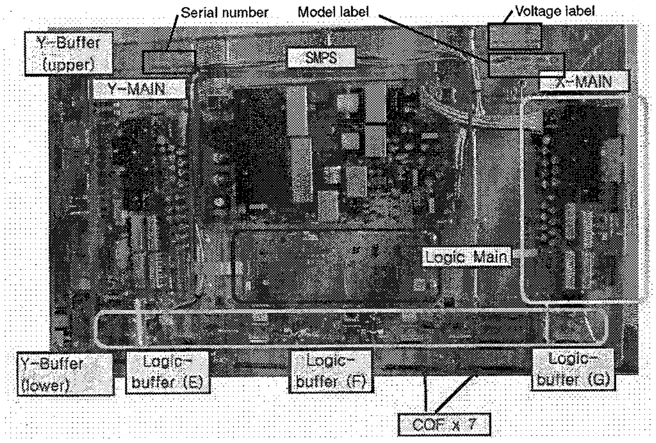
Serial number
Model label
Voltage label
Y-Buffer (upper)
SMPS
Y-MAIN
X-MAIN
Logic Main
Y-Buffer (lower)
Logic-buffer (E)
Logic-buffer (F)
Logic-buffer (G)
COF x 7

Figure 1-3 External view (42" SD v2)

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Figure 1-4 Points of screw mount (42" SD v2)

No	Item	Specification 42" SD v2	
1	Pixel	852 (H) x 480 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	2556 (H) x 480 (V)	
3	Pixel Pitch	1.095 mm (H) x 1.110 mm (V)	
4	Cell Pitch	R	0.324 (H) mm 1.110 (V) mm
		G	0.365 (H) mm 1.110 (V) mm
		B	0.406 (H) mm 1.110 (V) mm
5	Display size	932.940 (H) x 532.800(V) mm	
6	Screen size	Diagonal 42" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 52.9 (D) mm	
11	Weight	Module 1	About 16.6 kg
12	Broadc. reception Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.3 42" SD v3

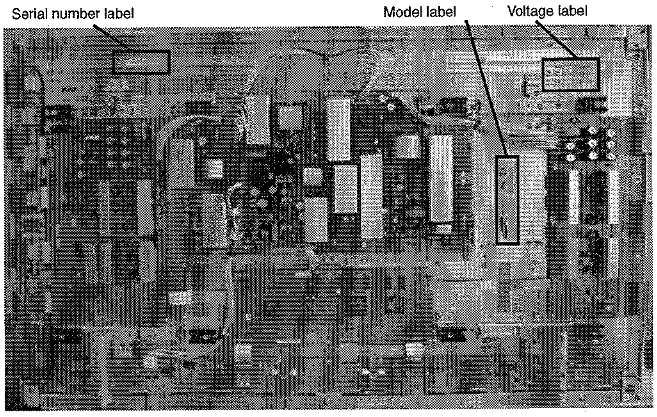
Serial number label
Model label
Voltage label

Figure 1-5 External view (42" SD v3)

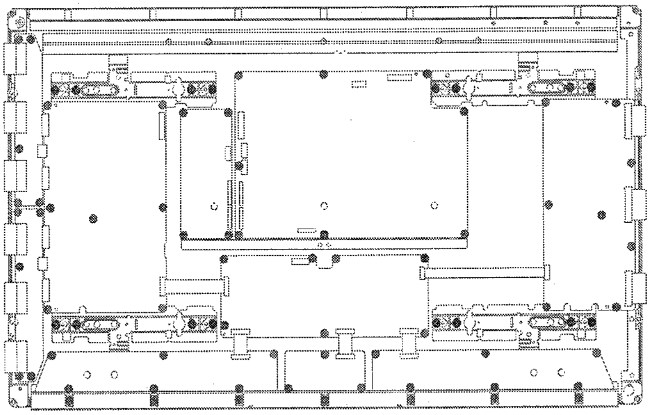

Figure 1-6 Points of screw mount (42" SD v3)

No	Item	Specification 42" SD v3	
1	Pixel	852 (H) x 480 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	2556 (H) x 480 (V)	
3	Pixel Pitch	1.095 mm (H) x 1.110 mm (V)	
4	Cell Pitch	R	0.365 (H) mm 1.110 (V) mm
		G	0.365 (H) mm 1.110 (V) mm
		B	0.365 (H) mm 1.110 (V) mm
5	Display size	932.940 (H) x 532.800(V) mm	
6	Screen size	Diagonal 42" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 52.9 (D) mm	
11	Weight	Module 1	About 16.6 kg
12	Broadc. reception Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.4 42" SD v4

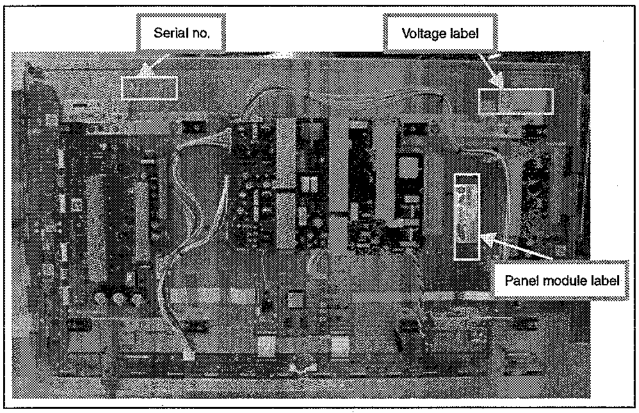

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Figure 1-7 External view (42" SD v4)

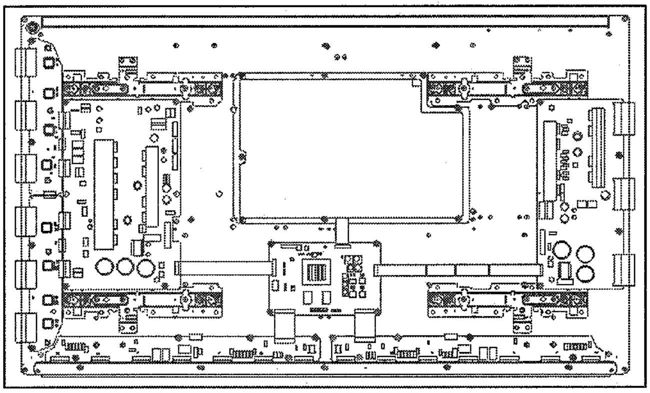

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Figure 1-8 Points of screw mount (42" SD v4)

No	Item	Specification 42" SD v4	
1	Pixel	852 (H) x 480 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	2556 (H) x 480 (V)	
3	Pixel Pitch	1.095 (H) mm x 1.110 (V) mm	
4	Cell Pitch	R	0.365 (H) mm x 1.110 (V) mm
		G	0.365 (H) mm x 1.110 (V) mm
		B	0.365 (H) mm x 1.110 (V) mm
5	Display size	932.940 (H) x 532.800(V) mm	
6	Screen size	Diagonal 42" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 54 (D) mm	
11	Weight	Module 1	About 15.4 kg
14	Broadc. reception Vertical frequency Video/Logic Interface	60 Hz/ 50 Hz, LVDS	

1.1.5 42" HD v3

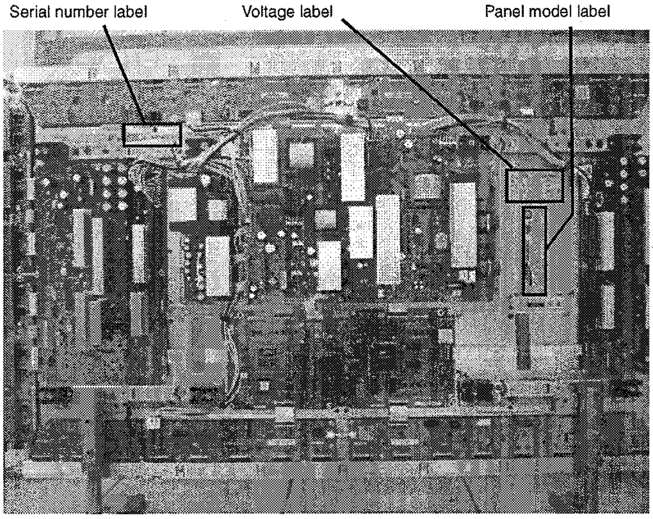

Figure 1-9 External view (42" HD v3)

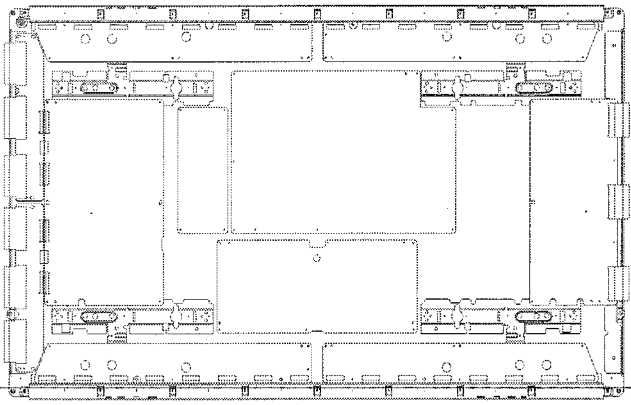

Figure 1-10 Points of screw mount (42" HD v3)

No	Item	Specification 42" HD v3	
1	Pixel	1.024 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	3072 (H) x 768 (V)	
3	Pixel Pitch	0.912mm (H) x 0.693mm (V)	
4	Cell Pitch	R	Horizontal 0.304 mm Vertical 0.693 mm
		G	Horizontal 0.304 mm Vertical 0.693 mm
		B	Horizontal 0.304 mm Vertical 0.693 mm
5	Display size	932.940 (H) x 532.800(V) mm	
6	Screen size	Diagonal 42" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 52.9 (D) mm	
11	Weight	Module 1	About 18.0 kg
12	Broadc. reception Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.6 42" HD v4

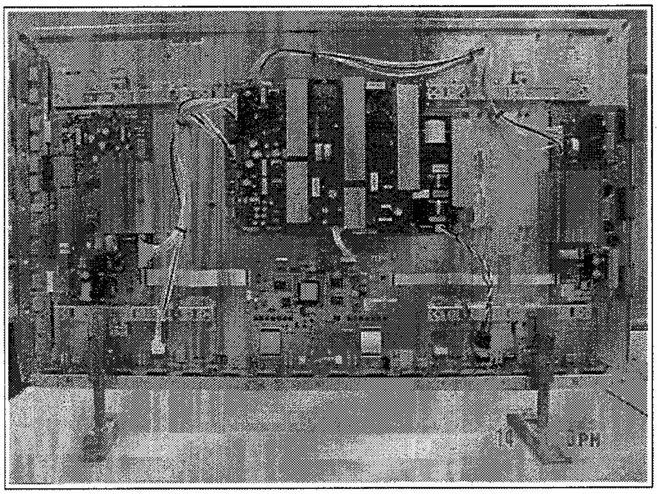

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Figure 1-11 External view (42" HD v4)

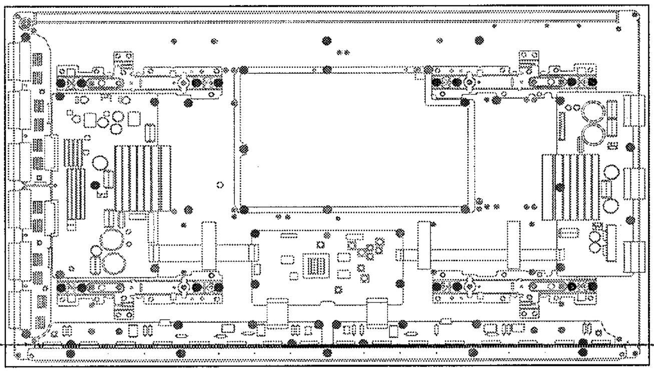

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Figure 1-12 Points of screw mount (42" HD v4)

No	Item	Specification 42" HD v4	
1	Pixel	1.024 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	3072 (H) x 768 (V)	
3	Pixel Pitch	0.912mm (H) x 1.110mm (V)	
4	Cell Pitch	R	Horizontal 0.304 mm Vertical 0.693 mm
		G	Horizontal 0.304 mm Vertical 0.693 mm
		B	Horizontal 0.304 mm Vertical 0.693 mm
5	Display size	933.98 (H) x 532.220(V) mm	
6	Screen size	Diagonal 42" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours (8-bit)	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	1000 (W) x 598 (H) x 64.4 (D) mm	
11	Weight	Module 1	About 20.0 kg
12	Broadc. reception Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.7 50" HD v3

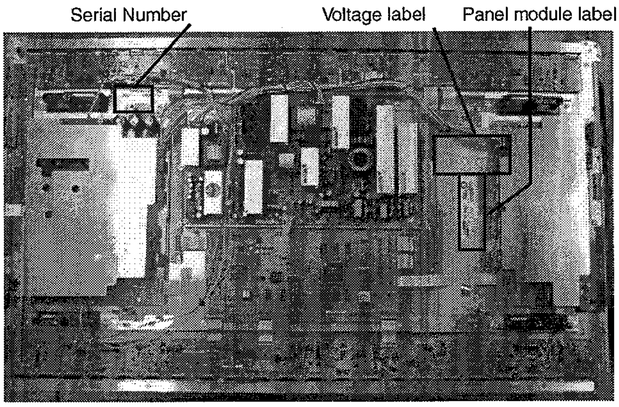

Figure 1-13 External view (50" HD v3)

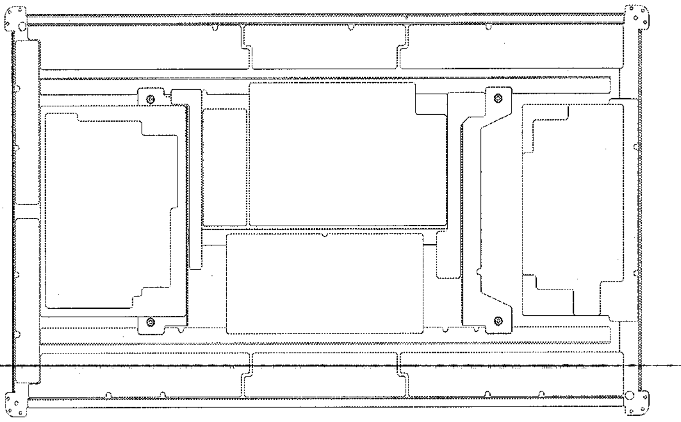

Figure 1-14 Points of screw mount (50" HD v3)

No	Item	Specification 50" HD v3	
1	Pixel	1366 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	4,098 (H) x 768 (V) cells	
3	Pixel Pitch	0.810mm (H) mm x 0.810 mm (V)	
4	Cell Pitch	R	Horizontal 0.270mm Vertical 0.810mm
		G	Horizontal 0.270mm Vertical 0.810mm
		B	Horizontal 0.270mm Vertical 0.810mm
5	Display size	1106.46 mm (H) x 622.08 mm (H)	
6	Screen size	Diagonal 50" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	1184 (W) x 700 (H) x 60.1 (D) mm	
11	Weight	Module 1	About 18.0 kg
12	Broadc. reception Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.8 50" HD v4

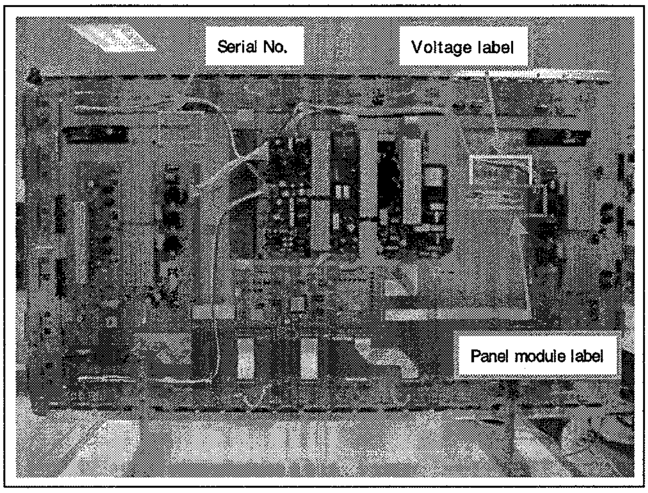
Serial No.
Voltage label
Panel module label

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Figure 1-15 External view (50" HD v4)

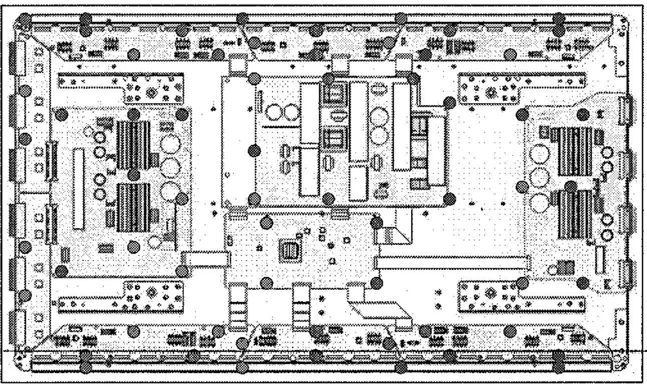

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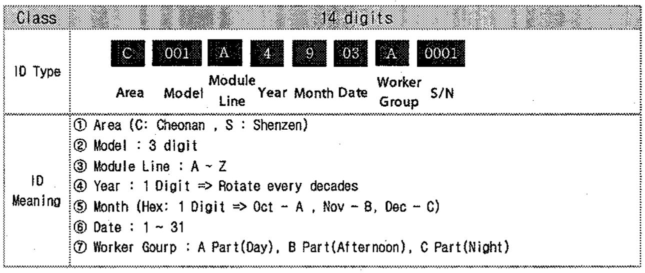
Figure 1-16 Points of screw mount (50" HD v4)

No	Item	Specification 50" HD v4	
1	Pixel	1366 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	4,098 (H) x 768 (V) cells	
3	Pixel Pitch	0.810mm (H) mm x 0.810 mm (V)	
4	Cell Pitch	R	Horizontal 0.270mm Vertical 0.810mm
		G	Horizontal 0.270mm Vertical 0.810mm
		B	Horizontal 0.270mm Vertical 0.810mm
5	Display size	1106.46 mm (H) x 622.08 mm (H)	
6	Screen size	Diagonal 50" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	1175 (W) x 682 (H) x 65.5 (D) mm	
11	Weight	Module 1	About 25.4 kg
12	Broadc. reception Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.2 Serial Numbers



Class	14 digits
ID Type	C 001 A 4 9 03 A 0001 Area Model Module Line Year Month Date Worker Group S/N
ID Meaning	① Area (C: Cheonan , S : Shenzen) ② Model : 3 digit ③ Module Line : A ~ Z ④ Year : 1 Digit => Rotate every decades ⑤ Month (Hex: 1 Digit => Oct - A , Nov - B, Dec - C) ⑥ Date : 1 ~ 31 ⑦ Worker Gourp : A Part(Day), B Part(Afternoon), C Part(Night)

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Figure 1-17 Module serial number

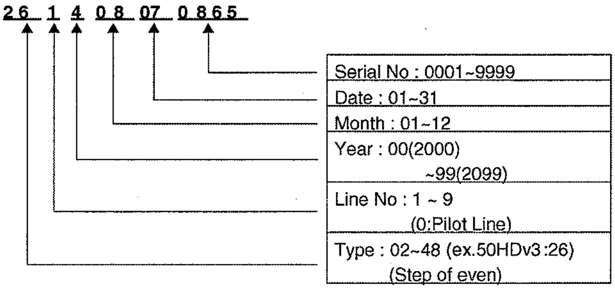
26 1 4 08 07 0865
Serial No : 0001~9999
Date : 01~31
Month : 01~12
Year : 00(2000) ~99(2099)
Line No : 1 ~ 9 (0:Pilot Line)
Type : 02~48 (ex.50HDv3:26) (Step of even)

Figure 1-18 Panel serial number

1.3 Chassis Overview

1.3.1 37" SD v4

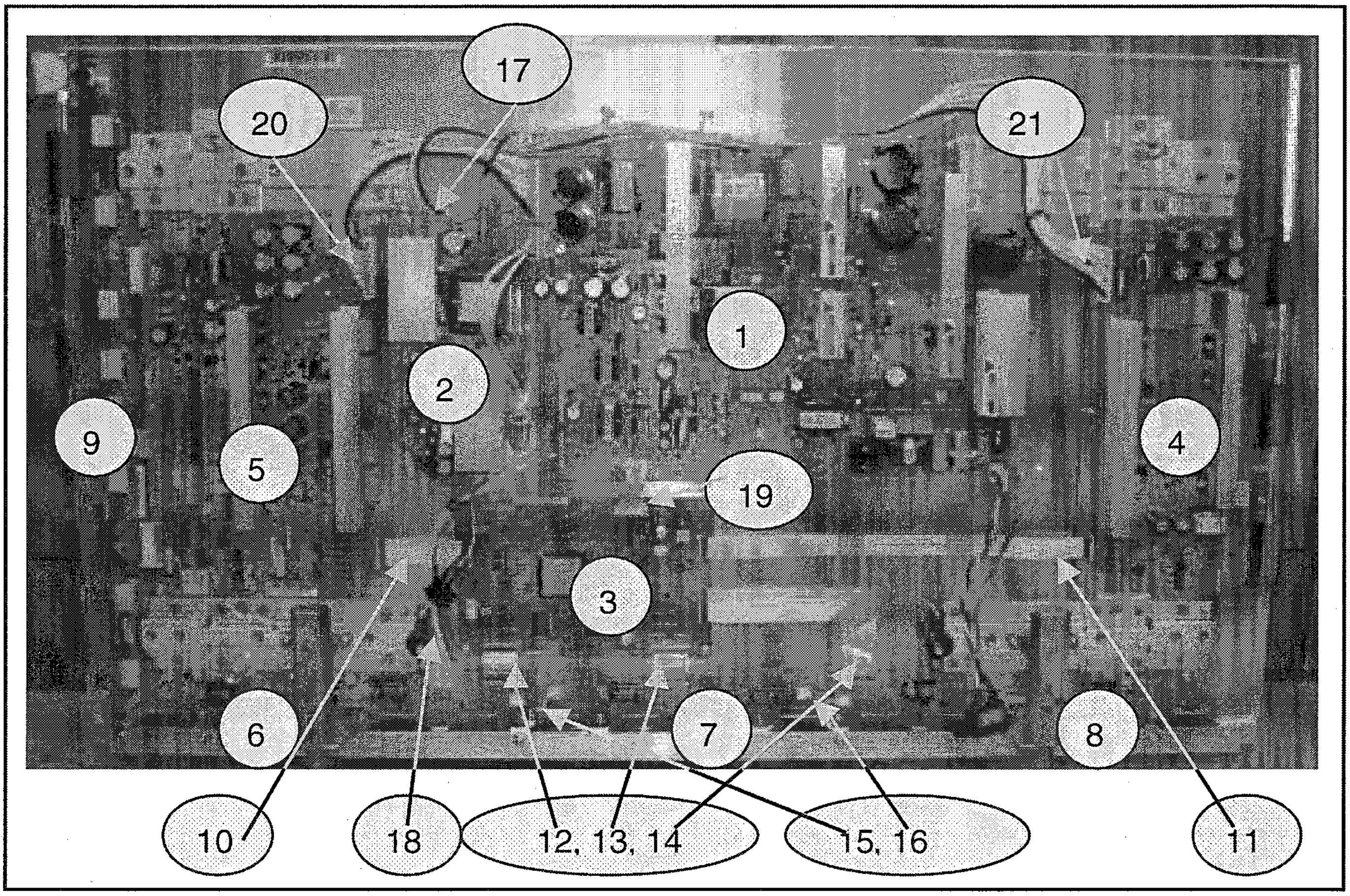

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Figure 1-19 PWB location (37" SD v4)

Table 1-3 PWB overview (37" SD v4)

No.	Location	Name
1	Main PSU	Assy PWB PSU
2	SUB-PSU	Assy PWB SUB-PSU
3	LOGIC-MAIN Board	Assy PWB LOGIC Main
4	X-MAIN Driving Board	Assy PWB X Main
5	Y-MAIN Driving Board	Assy PWBY Main
6	LOGIC E BUFFER Board	Assy PWB Buffer
7	LOGIC F BUFFER Board	Assy PWB Buffer
8	LOGIC G BUFFER Board	Assy PWB Buffer
9	Y-BUFFER Board	Assy PWB Buffer
10	LOGIC + Y-MAIN	FFC Cable-flat
11	LOGIC + X-MAIN	FFC Cable-flat
12	LOGIC + LOGIC BUF(E)	FFC Cable-flat
13	LOGIC + LOGIC BUF(F)	FFC Cable-flat
14	LOGIC + LOGIC BUF(G)	FFC Cable-flat
15	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
16	LOGIC BUF(F) + LOG. BUF(G)	Lead connector
17	PSU + SUB PSU	Lead connector
18	PSU + LOGIC BUF(E)	Lead connector
19	PSU + LOGIC MAIN	Lead connector
20	PSU + Y-MAIN	Lead connector

1.3.2 42" SD v2

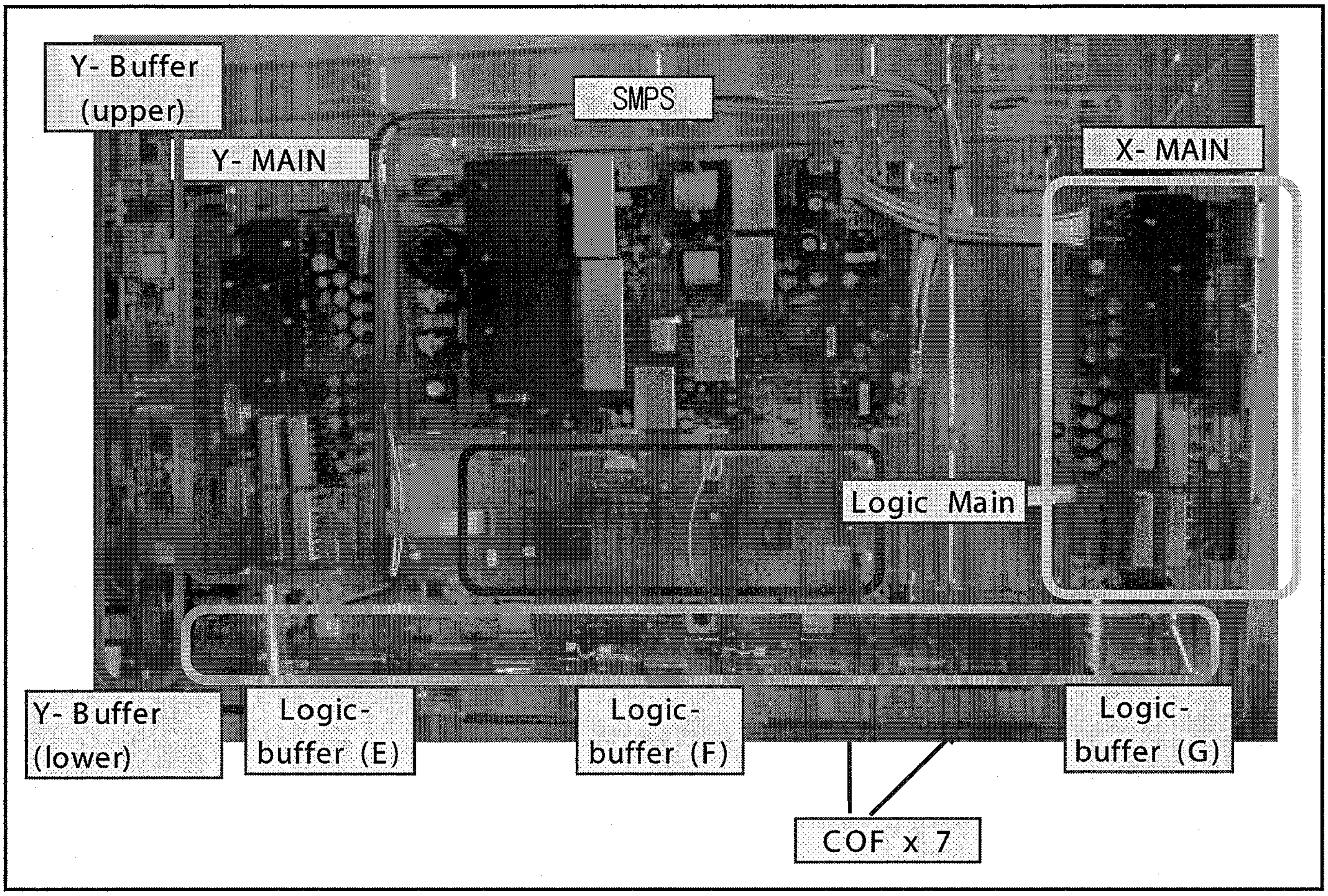
Y- Buffer (upper)
SMPS
Y- MAIN
X- MAIN
Logic Main
Y- Buffer (lower)
Logic- buffer (E)
Logic- buffer (F)
Logic- buffer (G)
COF x 7

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Figure 1-20 PWB location (42" SD v2)

Table 1-4 PWB overview (42" SD v2)

No.	Location	Name
1	info not available	
2		
3		
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21		
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23		

1.3.3 42" SD v3

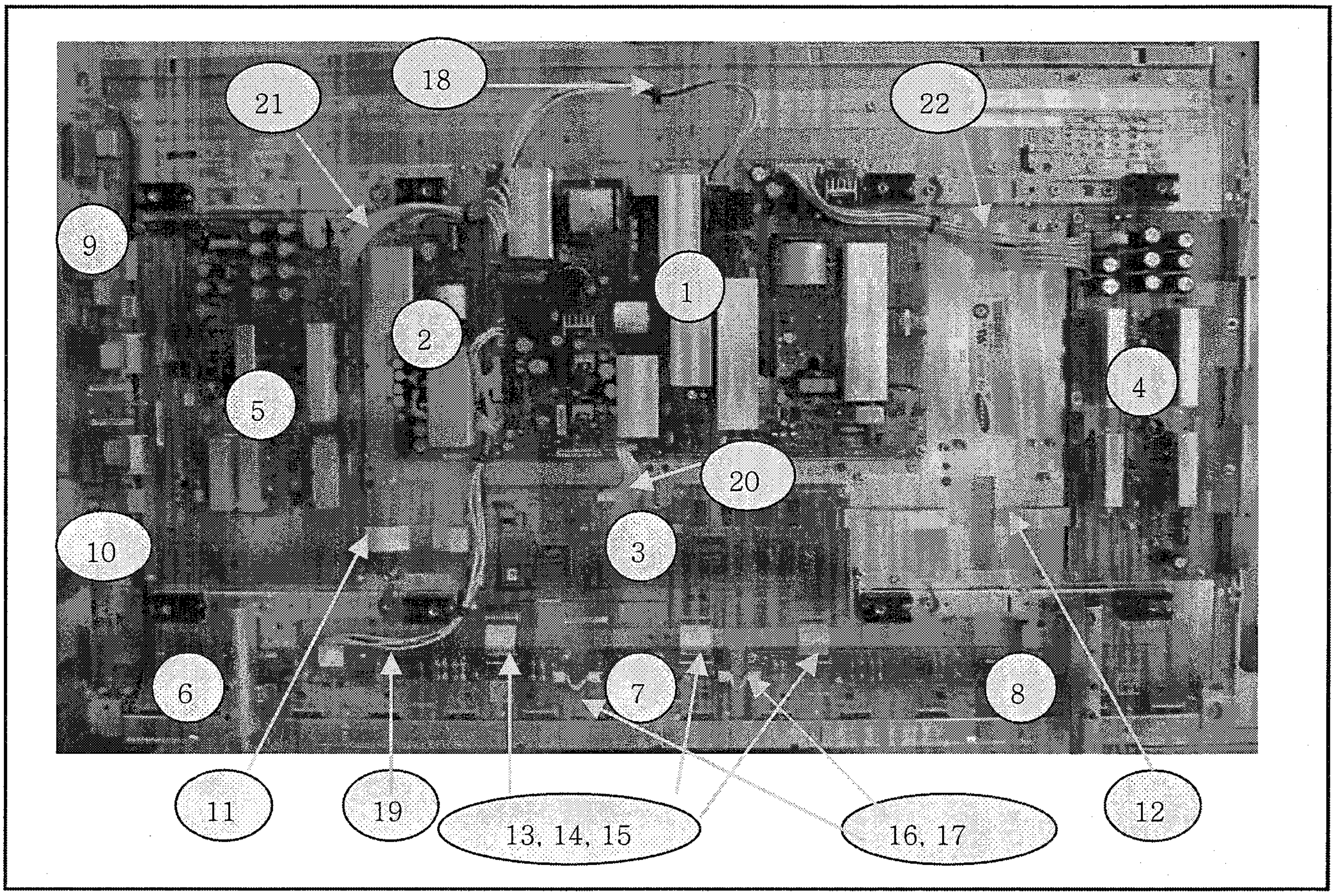

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Figure 1-21 PWB location (42" SD v3)

Table 1-5 PWB overview (42" SD v3)

No.	Location	Name
1	Main PSU	Assy PWB PSU
2	SUB-PSU	Assy PWB SUB-PSU
3	LOGIC-MAIN Board	Assy PWB LOGIC Main
4	X-MAIN Driving Board	Assy PWB X Main
5	Y-MAIN Driving Board	Assy PWBY Main
6	LOGIC E BUFFER Board	Assy PWB Buffer
7	LOGIC F BUFFER Board	Assy PWB Buffer
8	LOGIC G BUFFER Board	Assy PWB Buffer
9	Y-BUFFER (UPPER) Board	Assy PWB Buffer
10	Y-BUFFER (DOWN) Board	Assy PWB Buffer
11	LOGIC + Y-MAIN	FFC Cable-flat
12	LOGIC + X-MAIN	FFC Cable-flat
13	LOGIC + LOGIC BUF(E)	FFC Cable-flat
14	LOGIC + LOGIC BUF(F)	FFC Cable-flat
15	LOGIC + LOGIC BUF(G)	FFC Cable-flat
16	LOGIC BUF(E) +LOG. BUF(F)	Lead connector
17	LOGIC BUF(F) +LOG. BUF(G)	Lead connector
18	PSU + SUB PSU	Lead connector
19	PSU + LOGIC BUF(E)	Lead connector
20	PSU + LOGIC MAIN	Lead connector
21	PSU + Y-MAIN	Lead connector
22	PSU + X-MAIN	Lead connector

1.3.4 42" SD v4

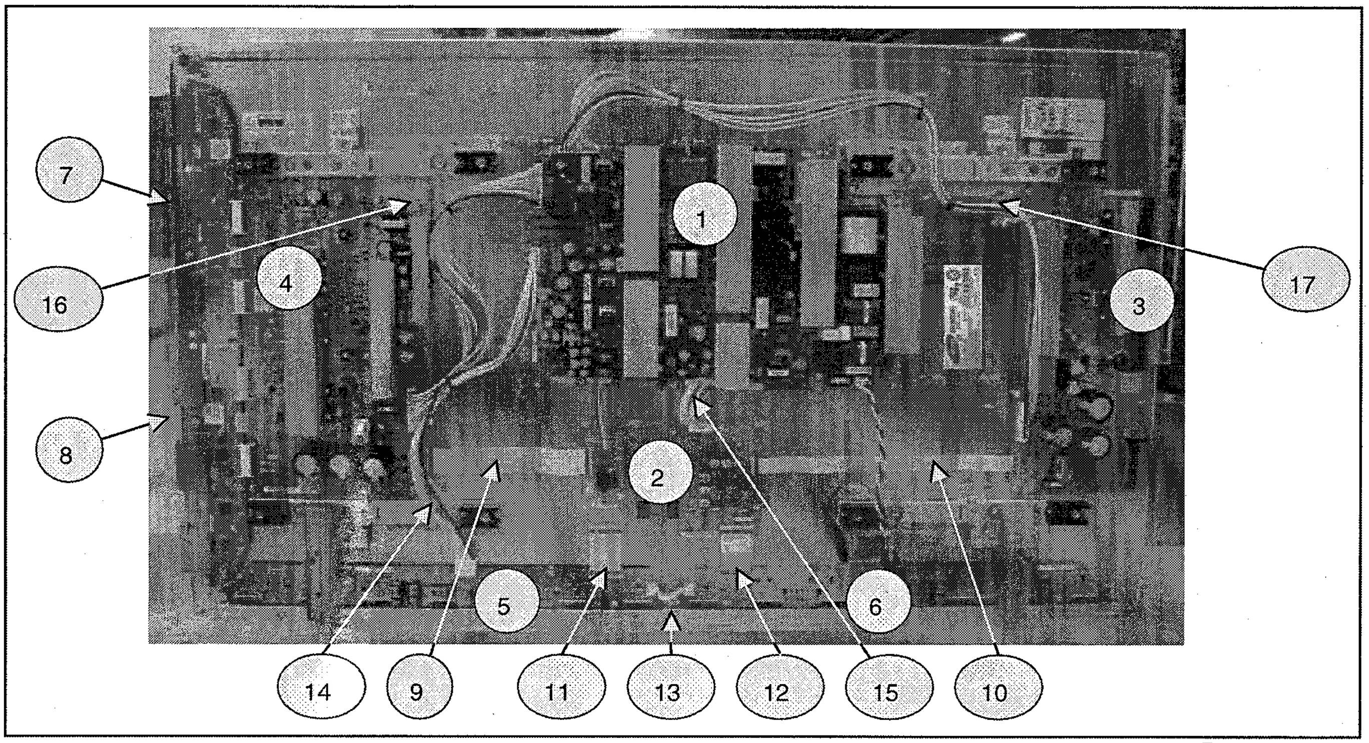

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Figure 1-22 PWB location (42" SD v4)

Table 1-6 PWB overview (42" SD v4)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWB Logic Main
3	X-MAIN Driving Board	Assy PWB X Main
4	Y-MAIN Driving Board	Assy PWB Y Main
5	LOGIC E BUFFER Board	Assy PWB buffer
6	LOGIC F BUFFER Board	Assy PWB buffer
7	Y-BUFFER (UPPER) Board	Assy PWB buffer
8	Y-BUFFER (DOWN) Board	Assy PWB buffer
9	LOGIC + Y-MAIN	FFC cable-flat
10	LOGIC + X-MAIN	FFC cable-flat
11	LOGIC + LOGIC BUF (E)	FFC cable-flat
12	LOGIC + LOGIC BUF (F)	FFC cable-flat
13	LOGIC BUF (E) + (F)	Lead connector
14	SMPS + LOGIC BUF (E)	Lead connector
15	SMPS + LOGIC MAIN	Lead connector
16	SMPS + Y-MAIN	Lead connector
17	SMPS + X-MAIN	Lead connector

1.3.5 42" HD v3

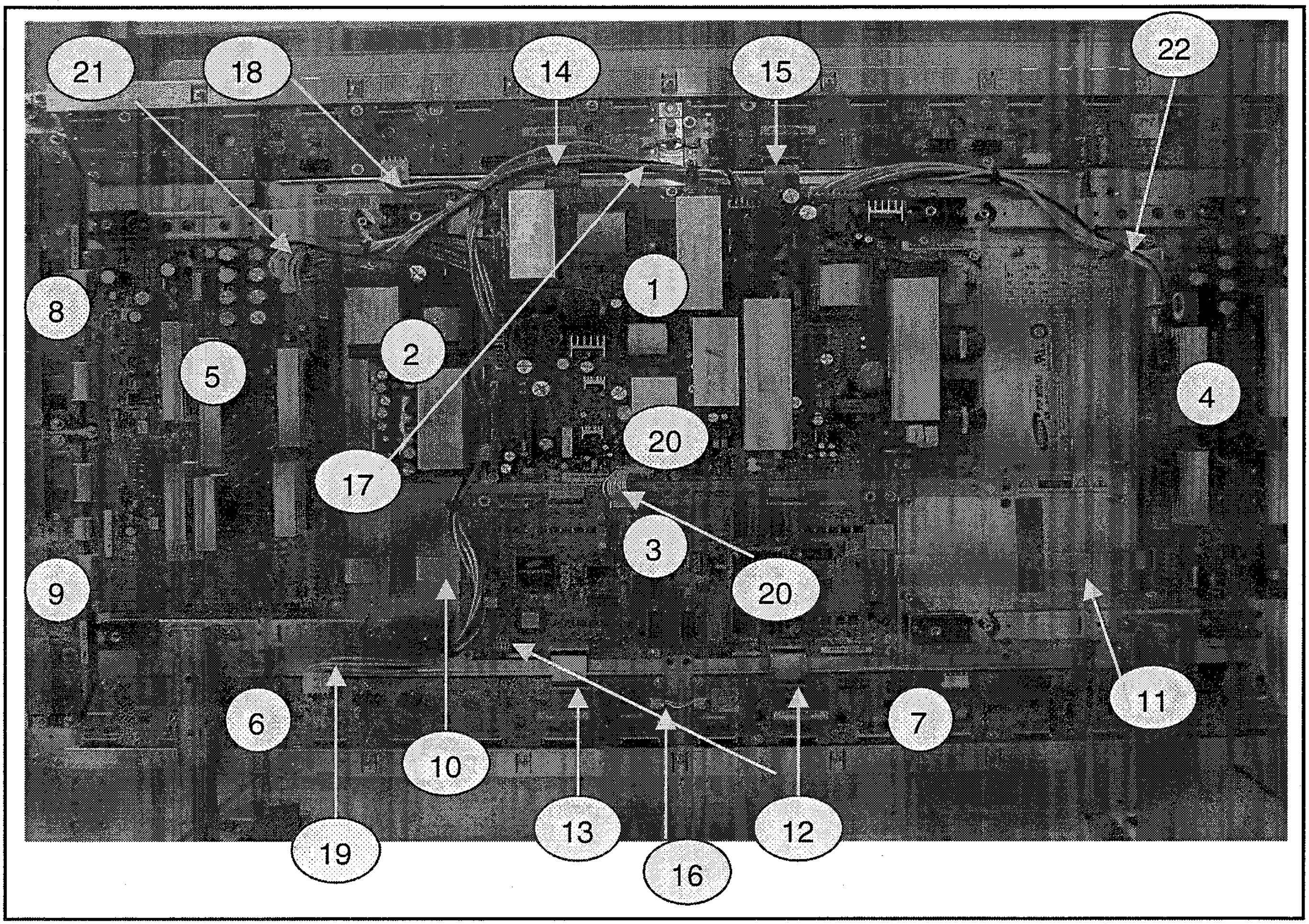

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Figure 1-23 PWB location (42" HD v3)

Table 1-7 PWB overview (42" HD v3)

No.	Location	Name
1	Main PSU	Assy PWB PSU
2	SUB-PSU	Assy PWB SUB-PSU
3	LOGIC-MAIN Board	Assy PWB LOGIC Main
4	X-MAIN Driving Board	Assy PWB X Main
5	Y-MAIN Driving Board	Assy PWB Y Main
6	LOGIC E BUFFER Board	Assy PWB Buffer
7	LOGIC F BUFFER Board	Assy PWB Buffer
8	Y-BUFFER (UPPER) Board	Assy PWB BuffeR
9	Y-BUFFER (DOWN) Board	Assy PWB Buffer
10	LOGIC + Y-MAIN	FFC Cable-flat
11	LOGIC + X-MAIN	FFC Cable-flat
12	LOGIC + LOG. BUF(E) (Down)	FFC Cable-flat
13	LOGIC + LOG. BUF(F) (Down)	FFC Cable-flat
14	LOGIC + LOGIC BUF(E) (Up)	FFC Cable-flat
15	LOGIC + LOGIC BUF(E) (Up)	FFC Cable-flat
16	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
17	PSU + SUB PSU	Lead connector
18	PSU + LOGIC BUF(E) (UP)	Lead connector
19	PSU + LOGIC BUF(E) (Down)	Lead connector
20	PSU + LOGIC MAIN	Lead connector
21	PSU + Y-MAIN	Lead connector
22	PSU + X-MAIN	Lead connector

1.3.6 42" HD v4

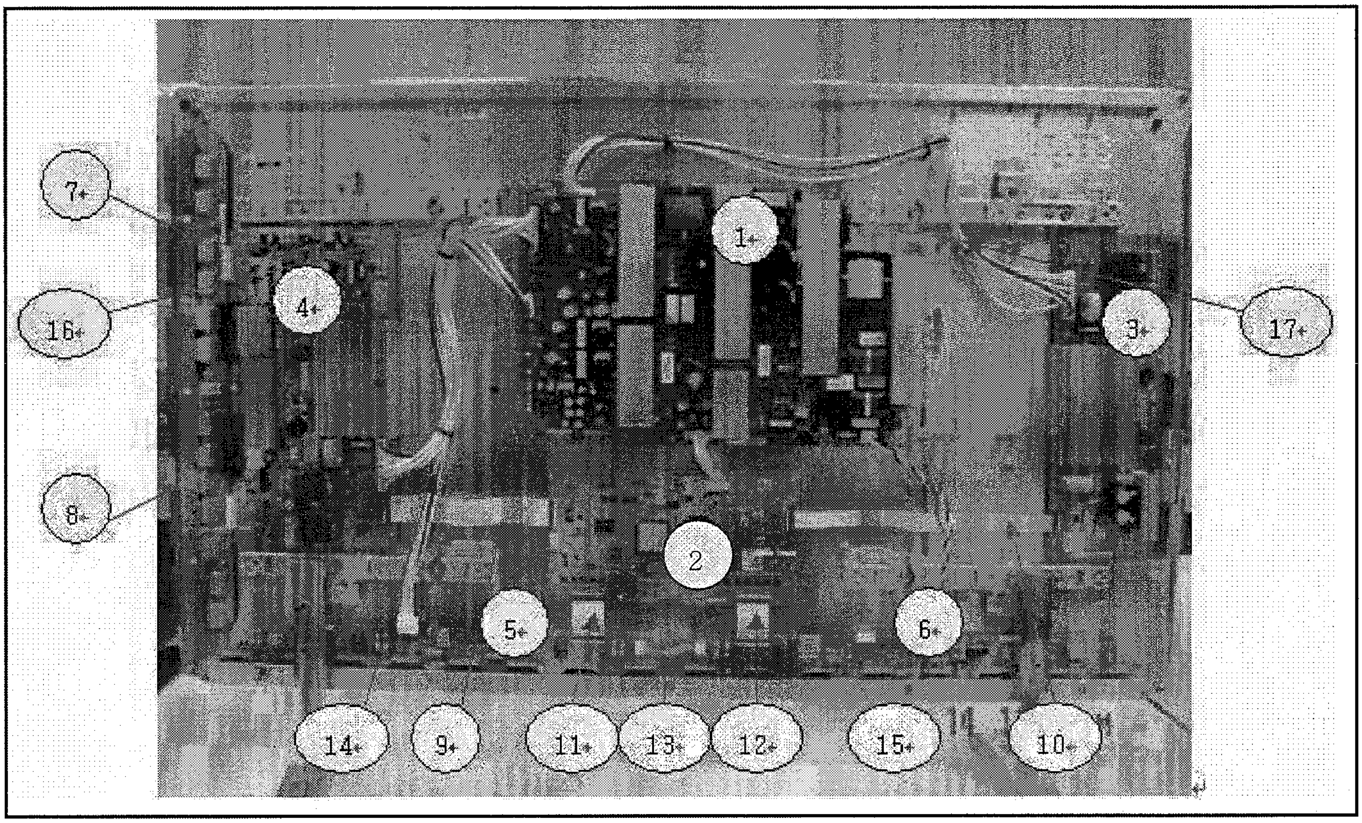

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Figure 1-24 PWB location (42" HD v4)

Table 1-8 PWB overview (42" HD v4)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWBLOGIC Main
3	X-MAIN Driving Board	Assy PWBX Main
4	Y-MAIN Driving Board	Assy PCBY Main
5	LOGIC E BUFFER Board	Assy PWB Buffer
6	LOGIC F BUFFER Board	Assy PWB Buffer
7	Y-BUFFER (UPPER) Board	Assy PWB Buffer
8	Y-BUFFER (DOWN) Board	Assy PWB Buffer
9	LOGIC + Y-MAIN	FFC Cable-flat
10	LOGIC + X-MAIN	FFC Cable-flat
11	LOGIC + LOGIC BUF(E)	FFC Cable-flat
12	LOGIC + LOGIC BUF(F)	FFC Cable-flat
13	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
14	SMPS + LOGIC BUF(E)	Lead connector
15	SMPS + LOGIC MAIN	Lead connector
16	SMPS + Y-MAIN	Lead connector
17	SMPS + X-MAIN	Lead connector

1.3.7 50" HD v3

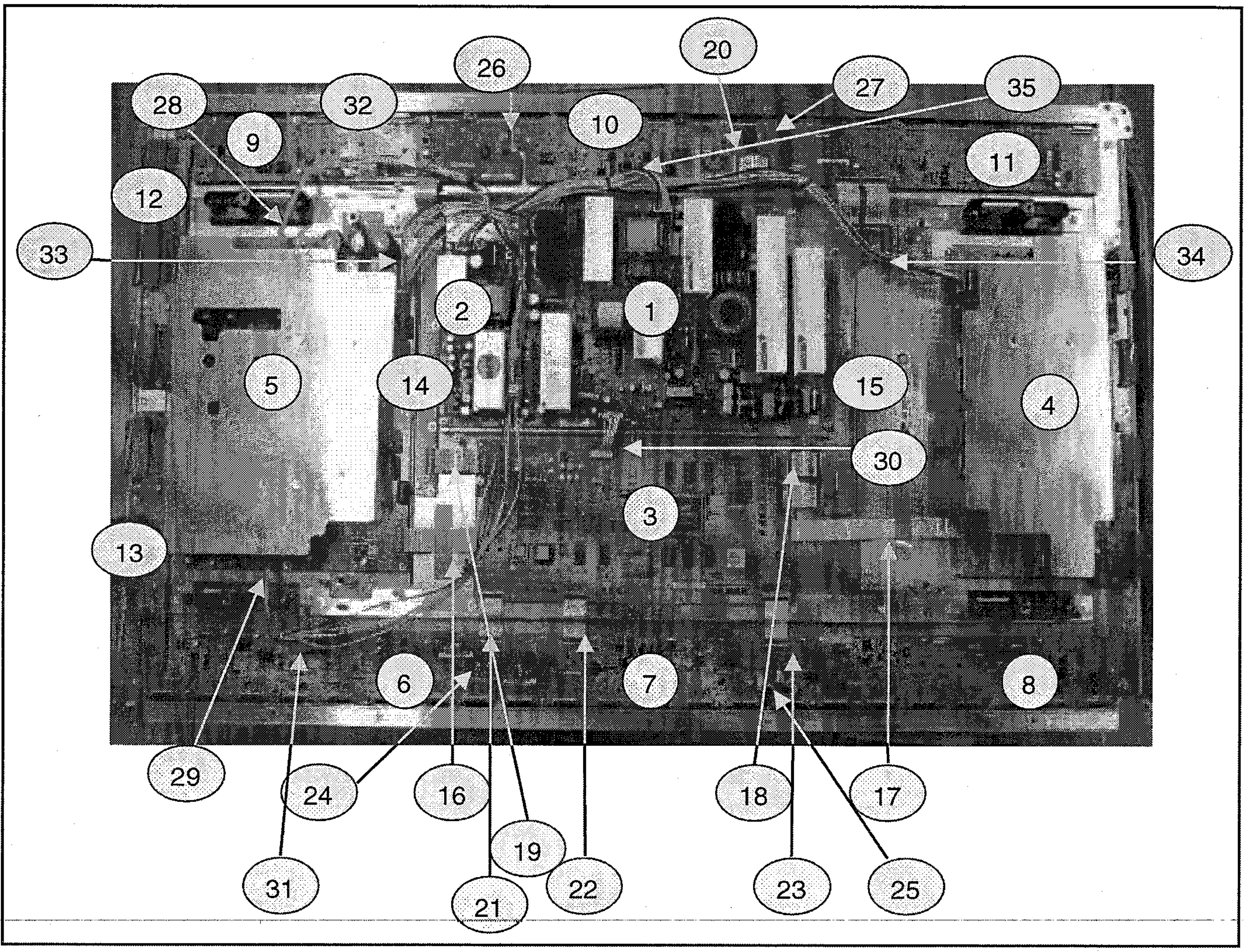

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Figure 1-25 PWB location (50" HD v3)

Table 1-9 PWB overview (50" HD v3)

No.	Location	Name
1	Main PUS	Assy PWBPSU
2	SUB-PSU	Assy PWBSUB-PSU
3	LOGIC-MAIN Board	Assy PWBLOGIC Main
4	X-MAIN Driving Board	Assy PWBX Main
5	Y-MAIN Driving Board	Assy PCBY Main
6	LOGIC E BUFFER Board	Assy PWB Buffer
7	LOGIC F BUFFER Board	Assy PWB Buffer
8	LOGIC G BUFFER Board	Assy PWB Buffer
9	LOGIC H BUFFER Board	Assy PWB Buffer
10	LOGIC I BUFFER Board	Assy PWB Buffer
11	LOGIC J BUFFER Board	Assy PWB Buffer
12	Y-BUFFER (UPPER) Board	Assy PWB Buffer
13	Y-BUFFER (DOWN) Board	Assy PWB Buffer
14	SUB-R	Assy PWB Buffer
15	SUB-L	Assy PWB Buffer
16	LOGIC + Y-MAIN	FFC Cable-flat
17	LOGIC + X-MAIN	FFC Cable-flat
18	SUB R + LOGIC	FFC Cable-flat
19	SUB L + LOGIC	FFC Cable-flat
20	LOG.BUF(I) + LOG.BUF(J) (Up)	FFC Cable-flat
21	LOGIC + LOG. BUF(E) (Down)	FFC Cable-flat
22	LOGIC + LOG. BUF(F) (Down)	FFC Cable-flat
23	LOGIC + LOG. BUF(G) (Down)	FFC Cable-flat
24	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
25	LOGIC BUF(F) + LOG. BUF(G)	Lead connector
26	LOGIC BUF(H) + LOG. BUF(I)	Lead connector
27	LOGIC BUF(I) + LOG. BUF(J)	Lead connector
28	Y-MAIN + LOGIC BUF(H)	Lead connector
29	Y-MAIN + LOGIC BUF(E)	Lead connector
30	PSU + LOGIC MAIN	Lead connector
31	PSU + LOGIC BUF(E)	Lead connector
32	PSU + LOGIC BUF(H)	Lead connector
33	PSU + Y-MAIN	Lead connector
34	PSU + X-MAIN	Lead connector
35	PSU + SUB PSU	Lead connector

1.3.8 50” HD v4

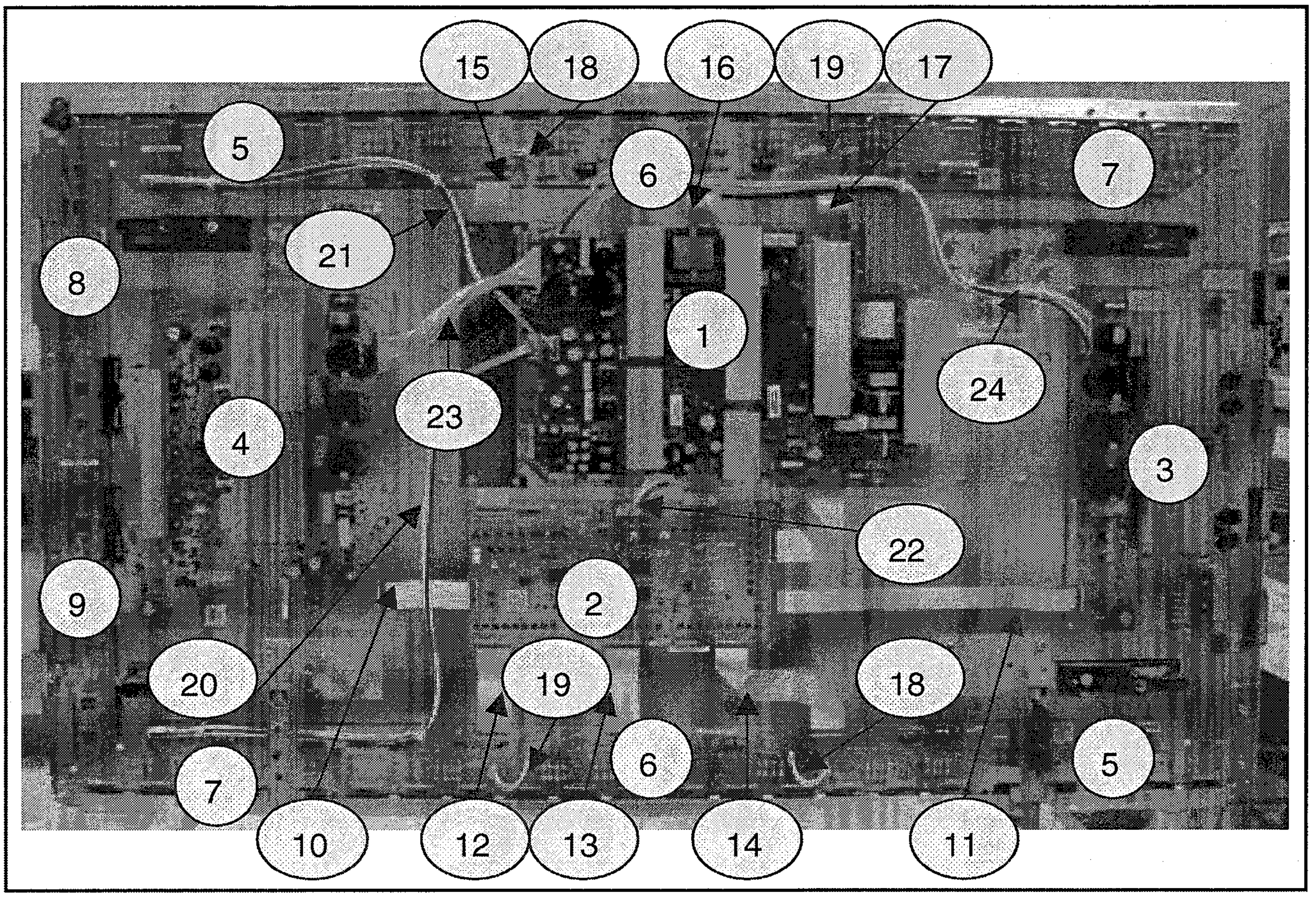

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Figure 1-26 PWB location (50” HD v4)

Table 1-10 PWB overview (50” HD v4)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWBLOGIC Main
3	X-MAIN Driving Board	Assy PWBX Main
4	Y-MAIN Driving Board	Assy PCBY Main
5	LOGIC E BUFFER Board	Assy PWB Buffer
6	LOGIC F BUFFER Board	Assy PWB Buffer
7	LOGIC G BUFFER Board	Assy PWB Buffer
8	Y-BUFFER (Upper) Board	Assy PWB Buffer
9	Y-BUFFER (Down) Board	Assy PWB Buffer
10	LOGIC + Y-MAIN	FFC Cable-flat
11	LOGIC + X-MAIN	FFC Cable-flat
12	LOGIC + LOG. BUF(G: Down)	FFC Cable-flat
13	LOGIC + LOG. BUF(F: Down)	FFC Cable-flat
14	LOGIC + LOG. BUF(E: Down)	FFC Cable-flat
15	LOGIC + LOG. BUF(E: Upper)	FFC Cable-flat
16	LOGIC + LOG. BUF(F: Upper)	FFC Cable-flat
17	LOGIC + LOG. BUF(G: Upper)	FFC Cable-flat
18	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
19	LOGIC BUF(F) + LOG. BUF(G)	Lead connector
20	SMPS + LOGIC BUF(G: Down)	Lead connector
21	SMPS + LOGIC BUF(E: Upper)	Lead connector
22	SMPS + LOGIC MAIN	Lead connector
23	SMPS + Y-MAIN	Lead connector
24	SMPS + X-MAIN	Lead connector

2. Safety Instructions, Warnings, and Notes

Index of this chapter:

2.1 Handling Precautions
2.2 Safety Precautions
2.3 Notes

Notes:

- Only authorised persons should perform servicing of this module.
- When using/handling this unit, pay special attention to the PDP Module: it should not be enforced into any other way then next rules, warnings, and/or cautions.
- "**Warning**" indicates a hazard that may lead to death or injury if the warning is ignored and the product is handled incorrectly.
- "**Caution**" indicates a hazard that can lead to injury or damage to property if the caution is ignored and the product is handled incorrectly.

2.1 Handling Precautions

- The PDP module use high voltage that is dangerous to humans. Before operating the PDP, always check for dust to prevent short circuits. Be careful touching the circuit device when power is "on".
- The PDP module is sensitive to dust and humidity. Therefore, assembling and disassembling must be done in no dust place.
- The PDP module has a lot of electric devices. The service engineer must wear equipment (for example, earth ring) to prevent electric shock and working clothes to prevent electrostatic.
- The PDP module use a fine pitch connector which is only working by exactly connecting with flat cable. The operator must pay attention to a complete connection when connector is reconnected after repairing.
- The capacitor's remaining voltage in the PDP module's circuit board temporarily remains after power is "off". Operator must wait for discharging of remaining voltage during at least 1 minute.

2.2 Safety Precautions

2.2.1 Safety Precautions

- Before replacing a board, discharge forcibly.
- The remaining electricity from board.
- When connecting FFC and TCPs to the module, recheck that they are perfectly connected.
- To prevent electrical shock, be careful not to touch leads during circuit operations.
- To prevent the Logic circuit from being damaged due to wrong working, do not connect/disconnect signal cables during circuit operations.
- Do thoroughly adjustment of a voltage label and voltage-insulation.
- Before reinstalling the chassis and the chassis assembly, be sure to use all protective stuff including a nonmetal controlling handle and the covering of partitioning type.
- Caution for design change: Do not install any additional devices to the module, and do not change the electrical circuit design.
- For example: Do not insert a subsidiary audio or video connector. If you insert It, it cause danger on safety. And, if you change the design or insert, manufacturer guarantee will be not effect.
- If any parts of wire is overheats of damaged, replace it with a new specified one immediately, and identify the cause of the problem and remove the possible dangerous factors.
- Examine carefully the cable status if it is twisted or damaged or displaced. Do not change the space between parts and circuit board. Check the cord of AC power preparing damage.
- Product Safety Mark: Some of electric or implement material have special characteristics invisible that was related on safety. In case of the parts are changed with new one, even though the Voltage and Watt is higher than before, the Safety and Protection function will be lost.
- The AC power always should be turned "off", before next repair.
- Check assembly condition of screw, parts and wire arrangement after repairing. Check whether the material around the parts get damaged.

2.2.2 ESD Precautions

There are parts, which are easily damaged by electrostatics (for example Integrated Circuits, FETs, etc.) Electrostatic damage rate of product will be reduced by the following technics:

- Before handling semiconductor parts/assembly, must remove positive electric by ground connection, or must wear the antistatic wrist-belt and ring (it must be operated after removing dust on it. It comes under precaution of electric shock).
- After removing the assembly, lay it with the tracks on a conductive surface to prevent charging.
- Do not use chemical stuff containing Freon. It generates positive electric that can damage ESD sensitive devices.
- You must use a soldering device for ground-tip when soldering or de-soldering these devices.
- You must use anti-static solder removal device. Most removal devices do not have antistatic which can charge a enough positive electric enough for damaging these devices.
- Before removing the protective material from the lead of a new device, bring the protective material into contact with the chassis or assembly.
- When handing an unpacked device for replacement, do not move around too much. Moving (legs on the carpet, for example) generates enough electrostatic to damage the device.
- Do not take a new device from the protective case until the it is ready to be installed. Most devices have a lead, which is easily short-circuited by conductive materials (such as conductive foam and aluminium)

2.3 Notes

A glass plate is positioned before the plasma display. This glass plate can be cleaned with a slightly humid cloth. If due to circumstances there is some dirt between the glass plate and the plasma display panel, it is recommended to do some maintenance by a qualified service employee only.

2.3.1 Safe PDP Handling

- The work procedures shown with the "Note" indication are important for ensuring the safety of the product and the servicing work. Be sure to follow these instructions.
- Before starting the work, secure a sufficient working space.
- At all times, other than when adjusting and checking the product, be sure to turn "off" the main POWER switch and disconnect the power cable from the power source of the display (jig or the display itself) during servicing.
- To prevent electric shock and breakage of PWBs, start the servicing work at least 30 seconds after the main power has been turned "off". Especially when installing and removing the Power Supply PWB and the SUS PWB in which high voltages are applied, start servicing at least 2 minutes after the main power has been turned "off".

- While the main power is "on", do not touch any parts or circuits other than the ones specified. The high voltage Power Supply block within the PDP module has a floating ground. If any connection other than the one specified is made between the measuring equipment and the high voltage power supply block, it can result in electric shock or activation of the leakage-detection circuit breaker.
- When installing the PDP module in, and removing it from the packing carton, be sure to have at least two persons perform the work while being careful to ensure that the flexible printed-circuit cable of the PDP module does not get caught by the packing carton.
- When the surface of the panel comes into contact with the cushioning materials, be sure to confirm that there is no foreign matter on top of the cushioning materials before the surface of the panel comes into contact with the cushioning materials. Failure to observe this precaution may result in, the surface of the panel being scratched by foreign matter.
- When handling the circuit PWB, be sure to remove static electricity from your body before handling the circuit PWB.
- Be sure to handle the circuit PWB by holding the large parts as the heat sink or transformer. Failure to observe this precaution may result in the occurrence of an abnormality in the soldered areas.
- Do not stack the circuit PWB. Failure to observe this precaution may result in problems resulting from scratches on the parts, the deformation of parts, and short-circuits due to residual electric charge.
- Routing of the wires and fixing them in position must be done in accordance with the original routing and fixing configuration when servicing is completed. All the wires are routed far away from the areas that become hot (such as the heat sink). These wires are fixed in position with the wire clamps so that the wires do not move, thereby ensuring that they are not damaged and their materials do not deteriorate over long periods of time. Therefore, route the cables and fix the cables to the original position and states using the wire clamps.
- Perform a safety check when servicing is completed. Verify that the peripherals of the serviced points have not undergone any deterioration during servicing. Also verify that the screws, parts and cables removed for servicing purposes have all been returned to their proper locations in accordance with the original

3. Directions For Use

Not applicable.

4. Mechanical Instructions

Index of this chapter:

4.1 Dis-assembling / Re-assembling
4.1.1 Flexible Printed Circuit of Y-Buffer (Upper and Lower)
4.1.2 Flat Cable Connector of X-main Board
4.1.3 FFC and TCP from Connector
4.1.4 Exchange of LBE, LBF, LBG board
4.1.5 Exchange YBU, YBL and YM board

4.1 Dis-assembling / Re-assembling

4.1.1 Flexible Printed Circuit of Y-Buffer (Upper and Lower)

- Dis-assembly: Pull out the FPC from the connector by holding the lead of the FPC with both hands.
- Re-assembly: Push the lead of FPC with same force on both sides into the connector.

Note: Be careful do not to damage the connector pin during connecting.

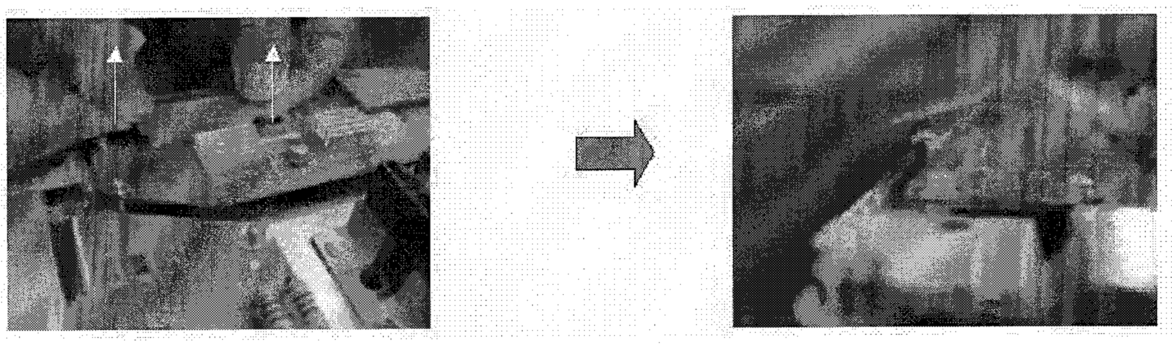


Figure 4-1 Dis-assembly FPC of Y-buffer

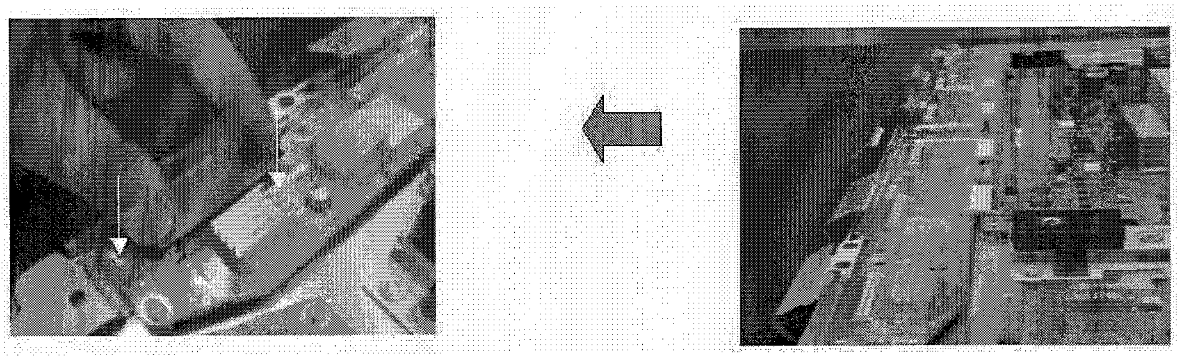


Figure 4-2 Re-assembly FPC of Y-buffer

4.1.2 Flat Cable Connector of X-main Board

- Dis-assembly:
  1. Pull out the clamp of connector.
  2. Pull Flat cable out press down lightly.
  3. Turn the Flat Cable reversely.
- Re-assembly: Put the Flat Cable into the connector press down lightly until locking sound ("Click") comes out.

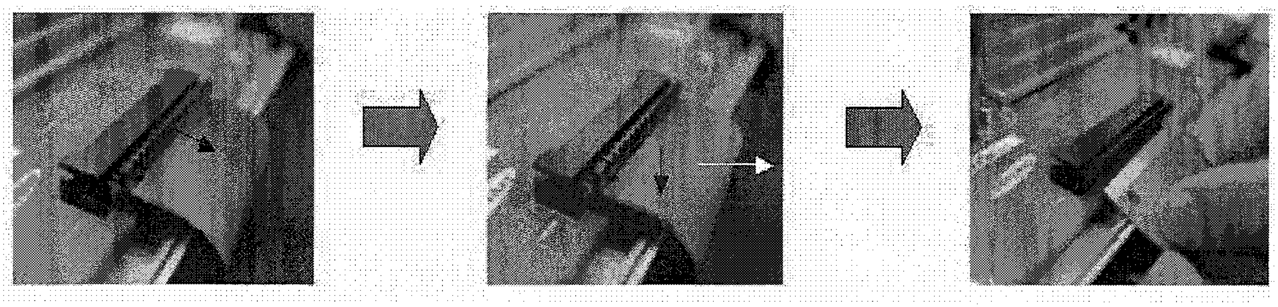


Figure 4-3 Dis-assembly FCC of X-main board

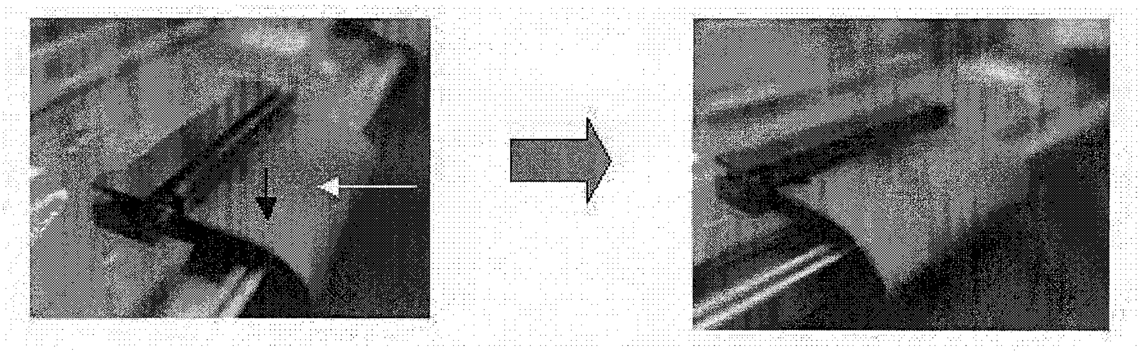


Figure 4-4 Re-assembly FCC of X-main board

4.1.3 *FFC and TCP from Connector*

- Dis-assembling of TCP:
  1. Open the clamp carefully.
  2. Pull the TCP out from its connector.
- Re-assembling of TCP:
  1. Put the TCP into the connector carefully
  2. Close the clamp completely (until "Click" comes out.).

Notes:

- Checking whether the foreign material is on the connector *inside before assembling of TCP.*
- Be careful, do not damage the board by ESD during handling of TCP.

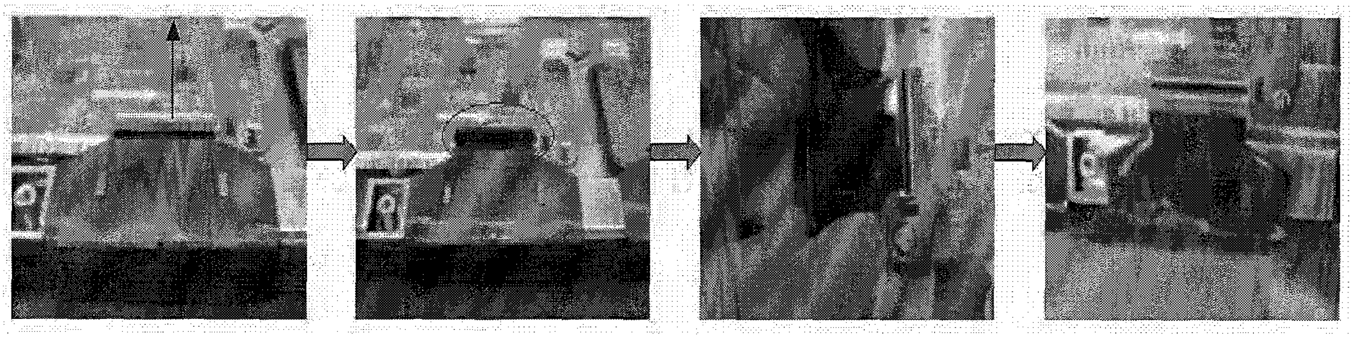


Figure 4-5 Dis-assembly of TCP

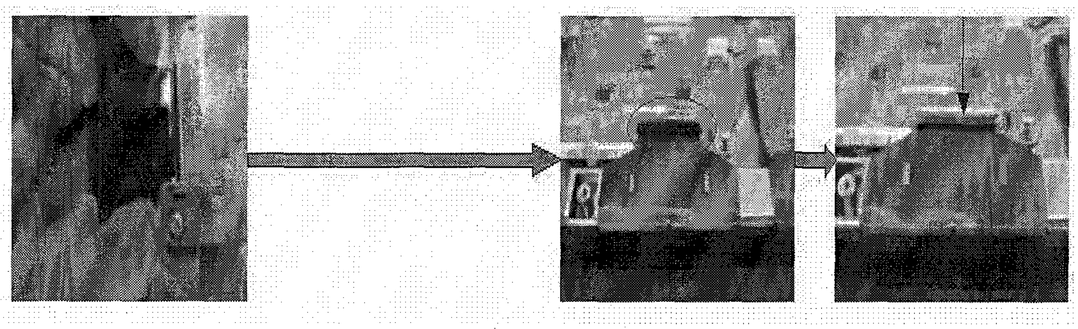


Figure 4-6 Re-assembly of TCP

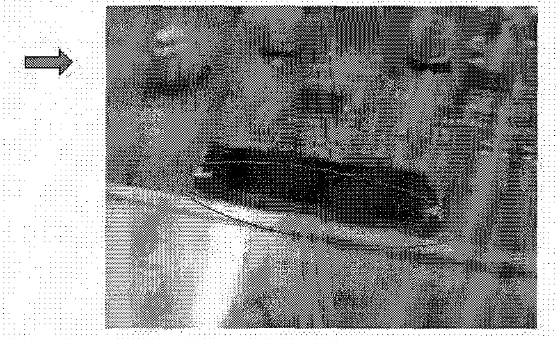
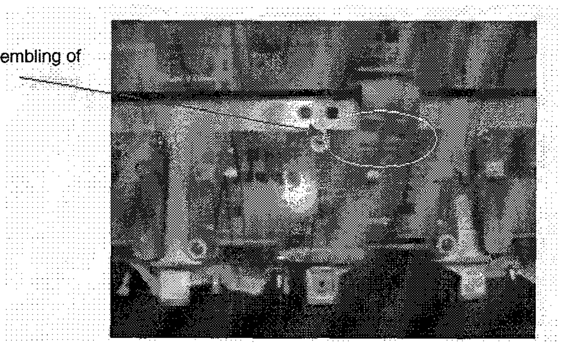


Figure 4-7 Mis-assembly of TCP



The procedure of assembling and disassembling of FFC is same as TCP

Figure 4-8 Dis- and re-assembly of FFC

4.1.4 Exchange of LBE, LBF, LBG board

1. Depending on the model (see "Photo 2" per model.):
   - **42" SD v3** - Remove the screws in order of 2-3-5-7-1-4-6 (and 10-11-13-16-9-12-14 for HD) from heat sink and then remove heat sink (Photo 1).
   - **42" SD v4** - Remove the screws in order of 2-4-1-5-3 from heat sink and then remove heat sink (Photo 1).
   - **42" HD v3, 37" SD v4, 50" HD v3** - Remove the screws in order of "Centre - Left Side - Right Side" from heat sink and then get rid of heat sink (Photo 1).
   - **50" HD v4** - Remove the screws in order of 2-3-1-4 from heat sink and then remove heat sink (Photo 1).
2. Remove the TPC, FFC, and power cable from the connectors.
3. Remove all the screws from the defective board.
4. Remove the defected board.
   Note: When replacing the Logic board or Y-main board for a lead-free (Pb-free) board, always replace them together. (this is **only** valid for the 37" SD v4 displays!)
5. Replace the new board and then screw tightly.
6. Clean the connectors.
7. Re-connect the TCP, FFC, and power cable to the connector.
8. Re-assemble the TCP heat sink. Use the same screw mounting order as described above

Caution: If you screw too tight, it is possible to damage the Driver IC of the TCP.

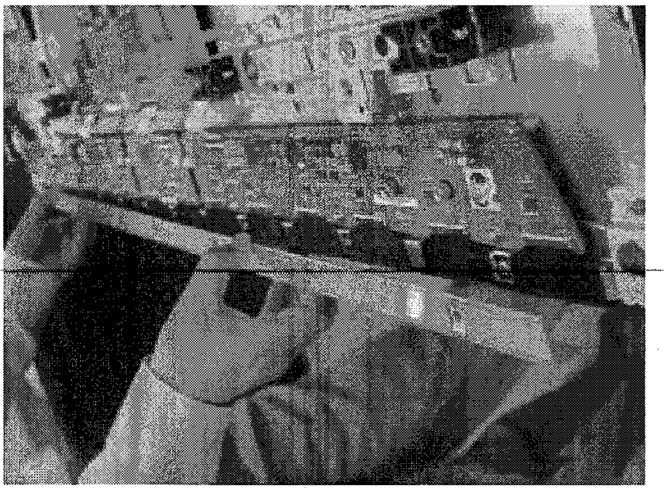


Figure 4-9 Photo 1 - Heatsink removal

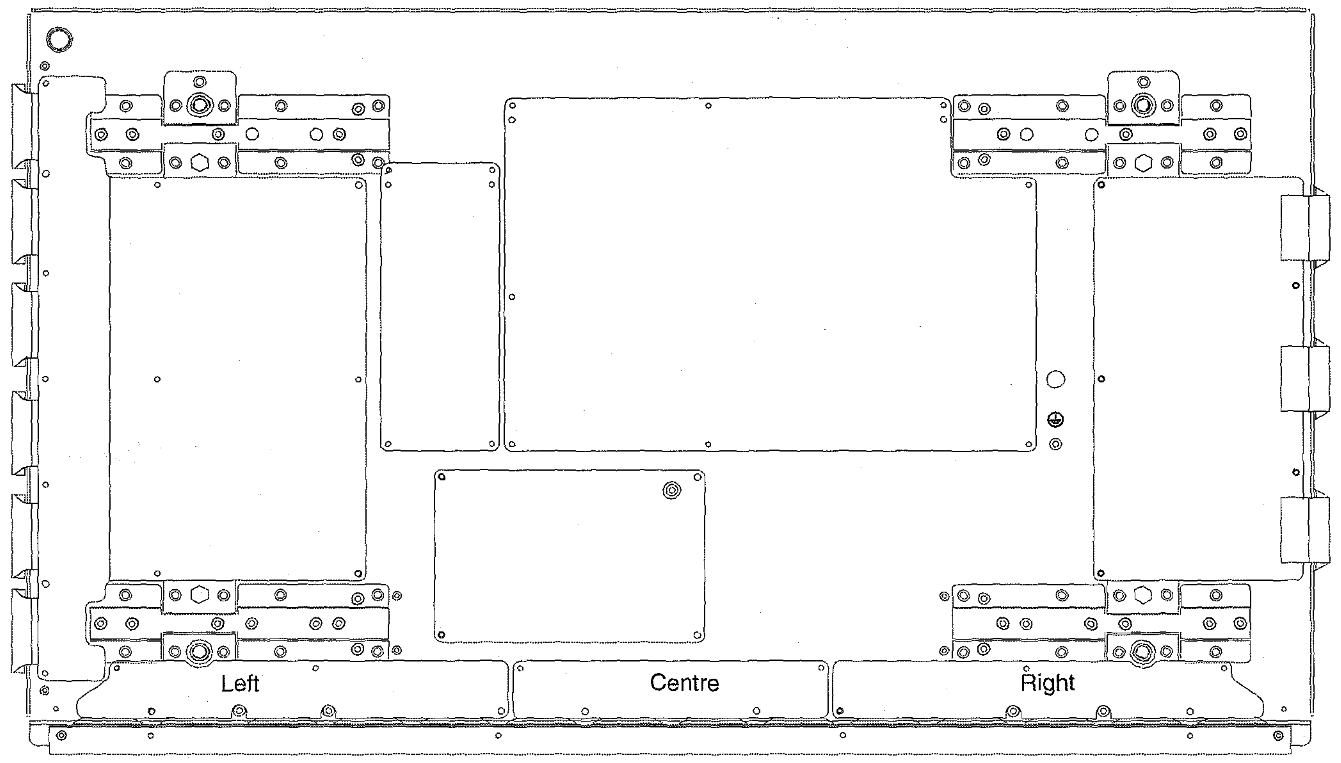

Left
Centre
Right

Figure 4-10 Photo 2 - 37" SD v4

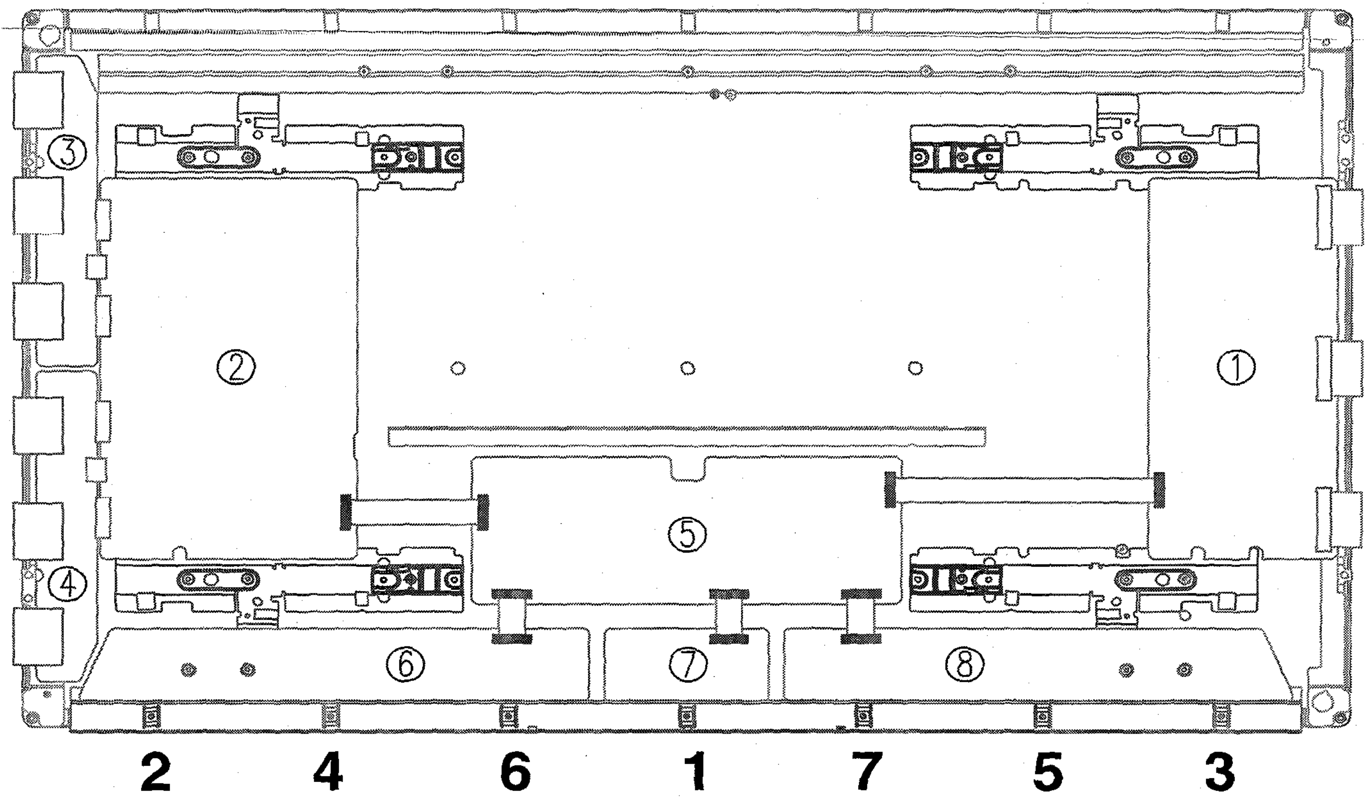

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Figure 4-11 Photo 2 - 42" SD v2 and v3

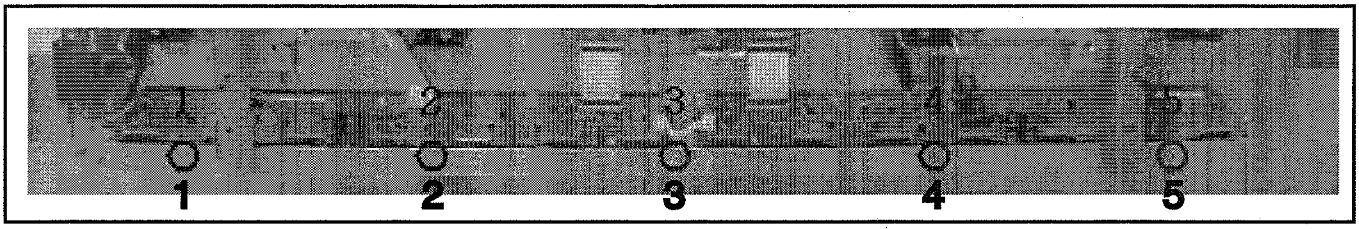

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Figure 4-12 Photo 2 - 42" SD v4

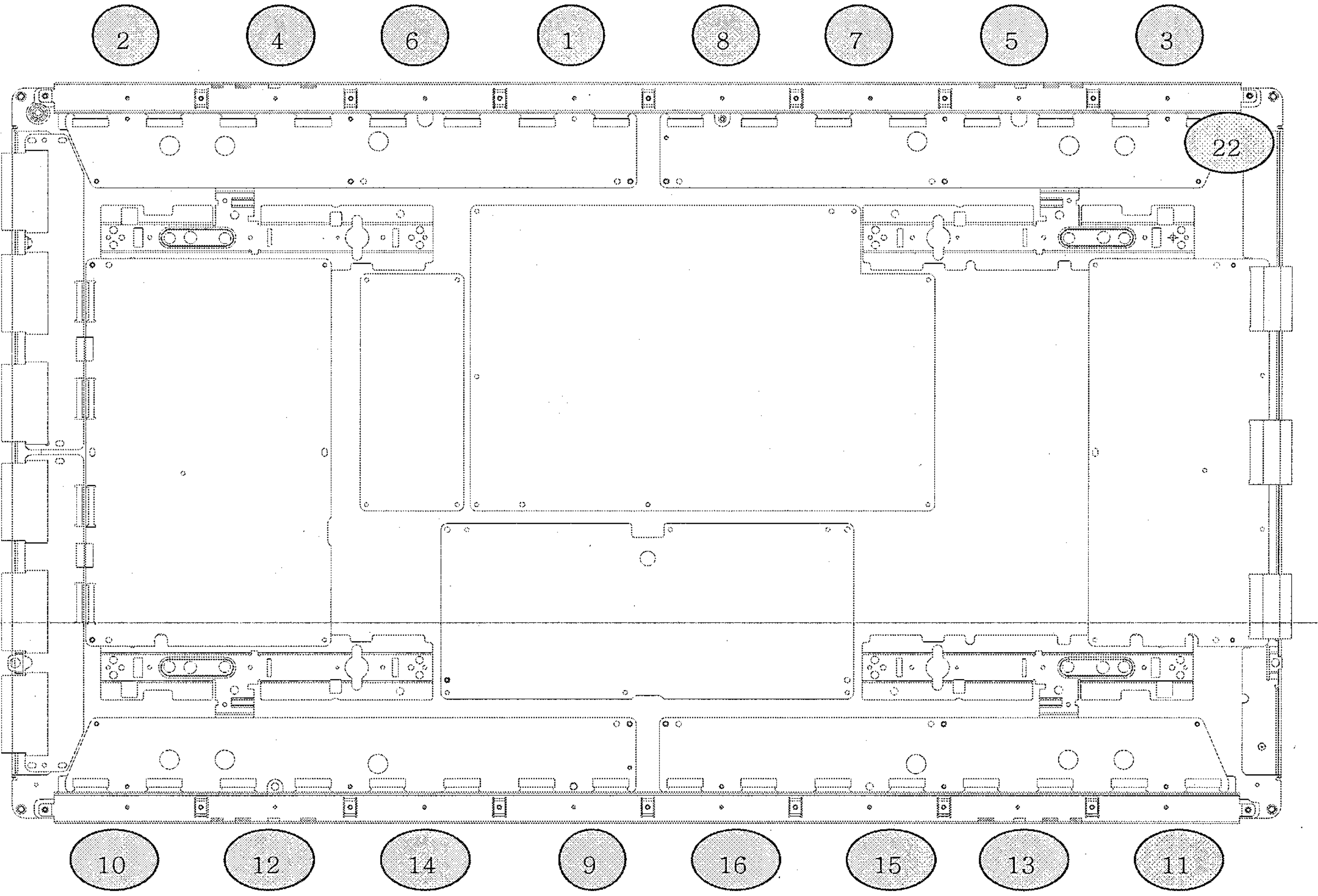
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Figure 4-13 Photo 2 - 42" HD v3

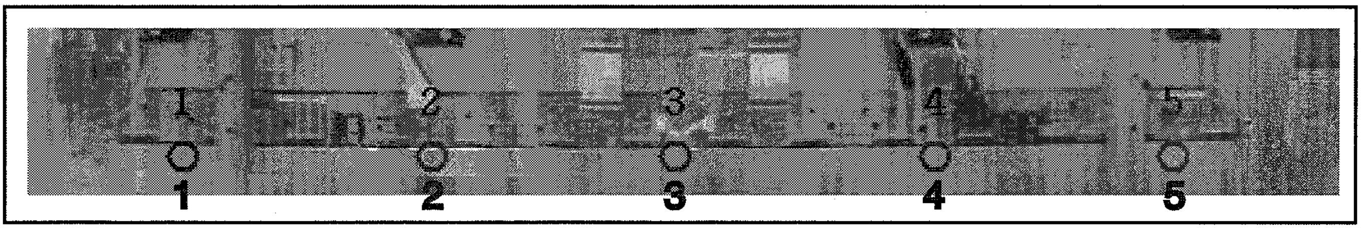

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Figure 4-14 Photo 2 - 42" HD v4

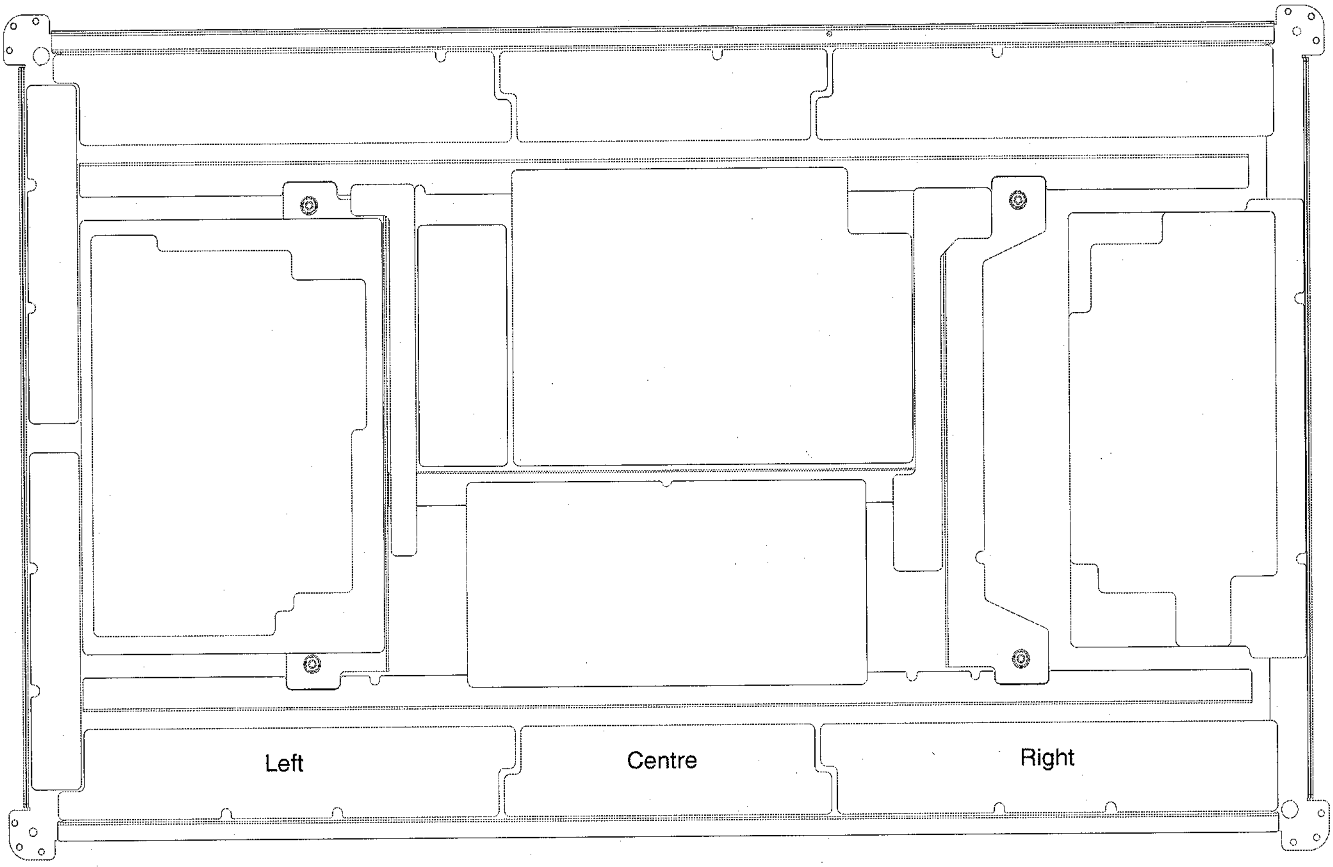
Left
Centre
Right

Figure 4-15 Photo 2 - 50” HD v3

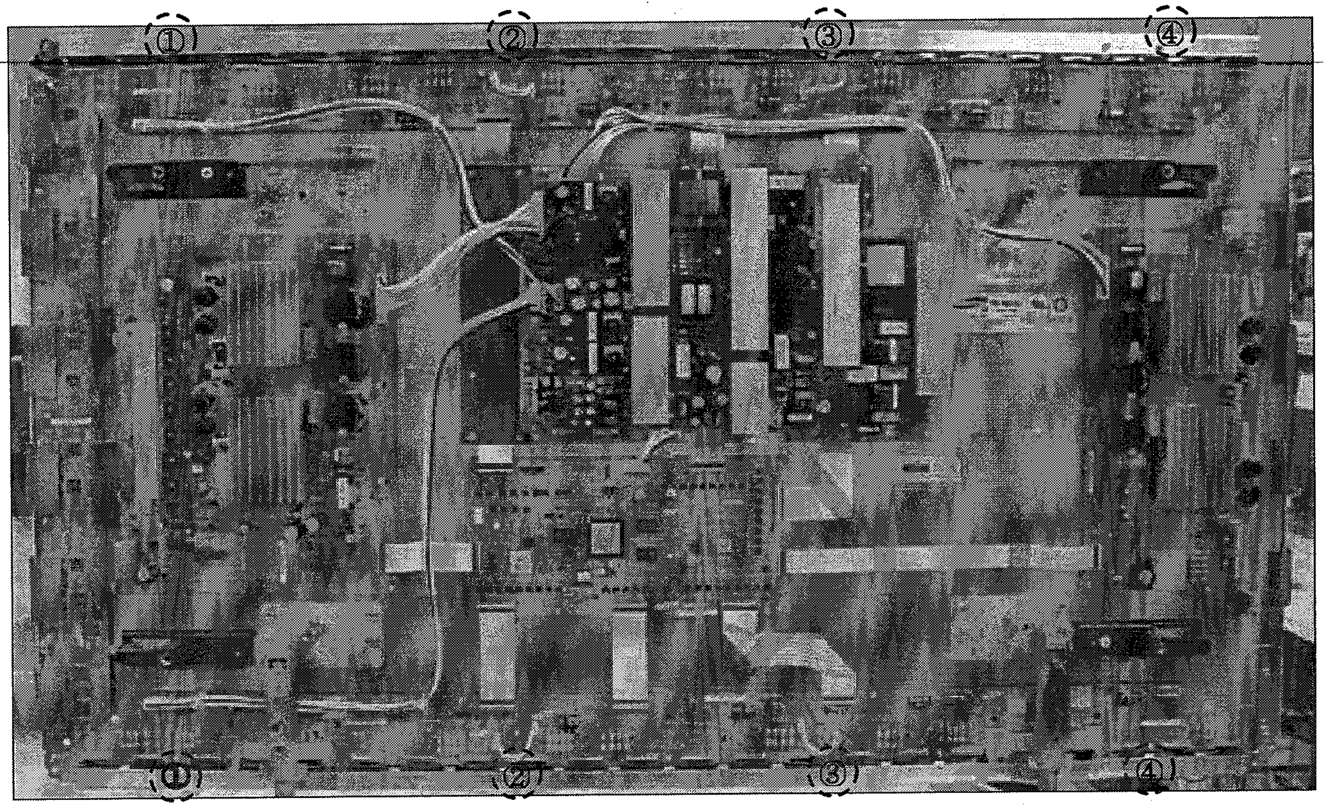

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Figure 4-16 Photo 2 - 50” HD v4

4.1.5 Exchange YBU, YBL and YM board

1. Separate all the FPC connector s of YBU (Y-Buffer upper) and YBL (Y-Buffer lower). See "Photo 1".
2. Separate all the connector of CN5001 and CN5008 from Y-Main. See "Photo 2".
3. Loosen all the screws of YBU, YBL, and YM. See "Photo 3".
4. Remove the board from chassis.
5. Remove the connector of CN5006 and CN5007 among YBU, YBL and YM.
6. Remove the YBL and YBU from Y-main.
7. Remove the defected board.
   Note: When replacing the Logic board or Y-main board for a lead-free (Pb-free) board, always replace them together. (this is **only** valid for the 37" SD v4 displays!)
8. Re-assemble the YBU and YBL to the Y-Main.
9. Connect the connector of CN5006 and CN5007 among YBU, YBL and YM. See "Photo 4".
10. Arrange the board on the chassis and then screw to fix.
11. Connect the FPC and YM of panel to the connector. See "Photo 5".
12. Supply the electric power to the module and then check the waveform of the board.
13. Turn "off" the power after the waveform is adjusted.

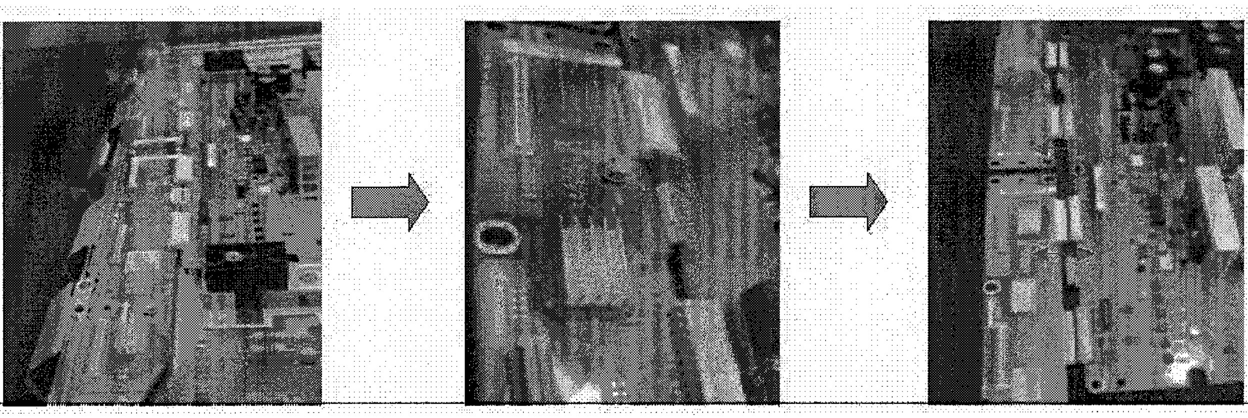


Figure 4-17 Photo 1, 2, and 3: Dis-assembly of YBU, YBL, and YM

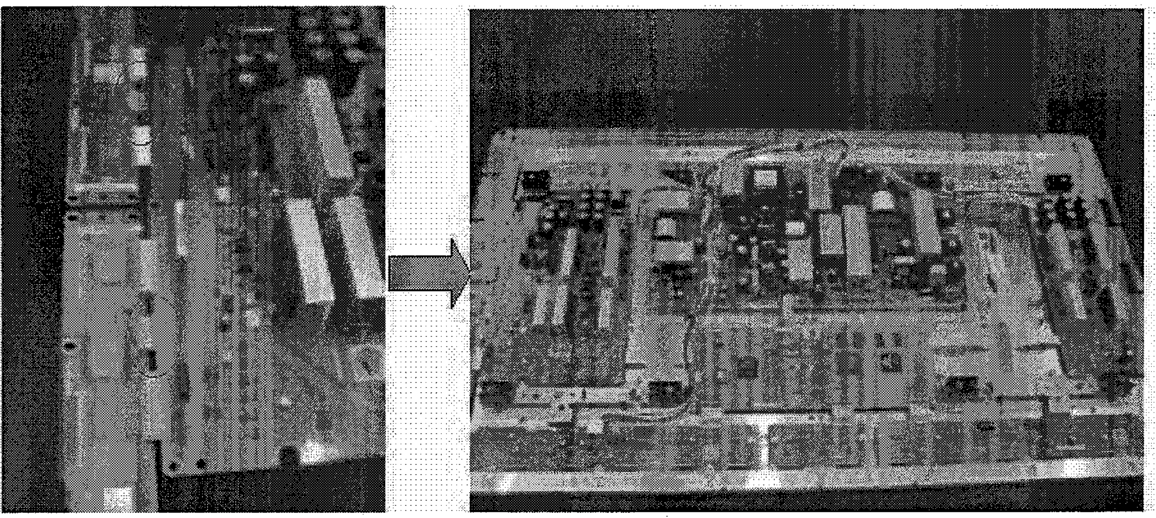


Figure 4-18 Photo 4 and 5: Re-assembly of YBU, YBL, and YM

5. Service Modes, Error Codes, and Fault Finding

Index of this chapter:

5.1 Repair Tools
5.2 Fault Finding
5.3 Defect Description Form

5.1 Repair Tools

5.1.1 ComPair

For the v3 and v4 models, it will be possible to generate test patterns with ComPair. The ComPair interface must be connected to the Logic Board with the special interconnection cable (see table below for the order code).

5.1.2 Other Service Tools

Table 5-1 Overview Service tools

Service Tools	Order Code
Jumper J8002 + V2 JIG connector kit	3122 785 90760
V3 JIG connector + for SDI panel repair	3122 785 90770
Jumper J8002 to be used in connector kit	3122 785 90780
V2 JIG connector to be used in conn. kit	3122 785 90790
ComPair / SDI interconnection cable	3122 785 90800
Foam buffers (2 pcs.)	3122 785 90581

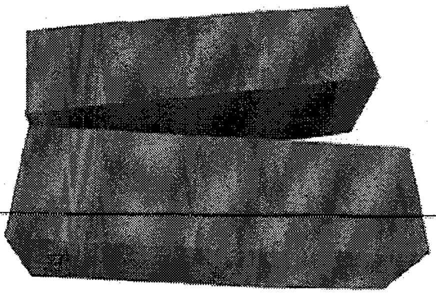
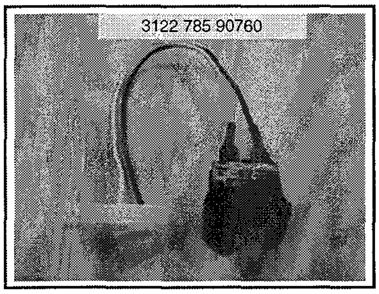


Figure 5-1 Foam buffers



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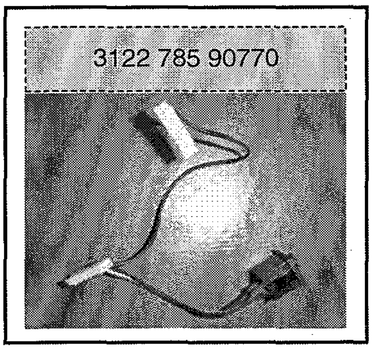
030805

Figure 5-2 V2 jig



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030805

Figure 5-3 V3 jig

5.2 Fault Finding

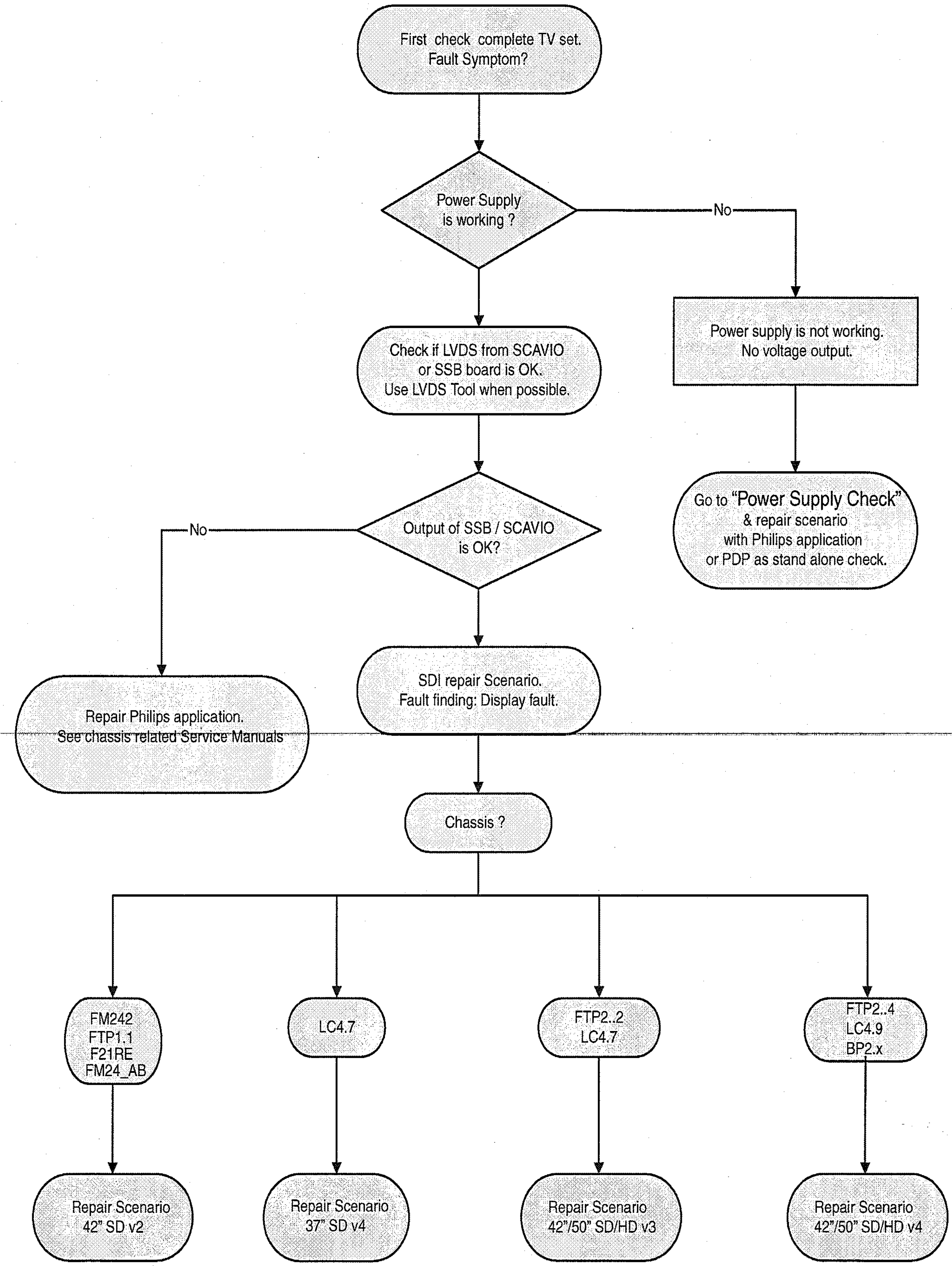
First check complete TV set.
Fault Symptom?
Power Supply
is working ?
No
Power supply is not working.
No voltage output.
Go to "Power Supply Check"
& repair scenario
with Philips application
or PDP as stand alone check.
Check if LVDS from SCAVIO
or SSB board is OK.
Use LVDS Tool when possible.
Output of SSB / SCAVIO
is OK?
No
Repair Philips application.
See chassis related Service Manuals
SDI repair Scenario.
Fault finding: Display fault.
Chassis ?
FM242
FTP1.1
F21RE
FM24_AB
LC4.7
FTP2..2
LC4.7
FTP2..4
LC4.9
BP2.x
Repair Scenario
42" SD v2
Repair Scenario
37" SD v4
Repair Scenario
42"/50" SD/HD v3
Repair Scenario
42"/50" SD/HD v4

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Figure 5-4 Which repair scenario?

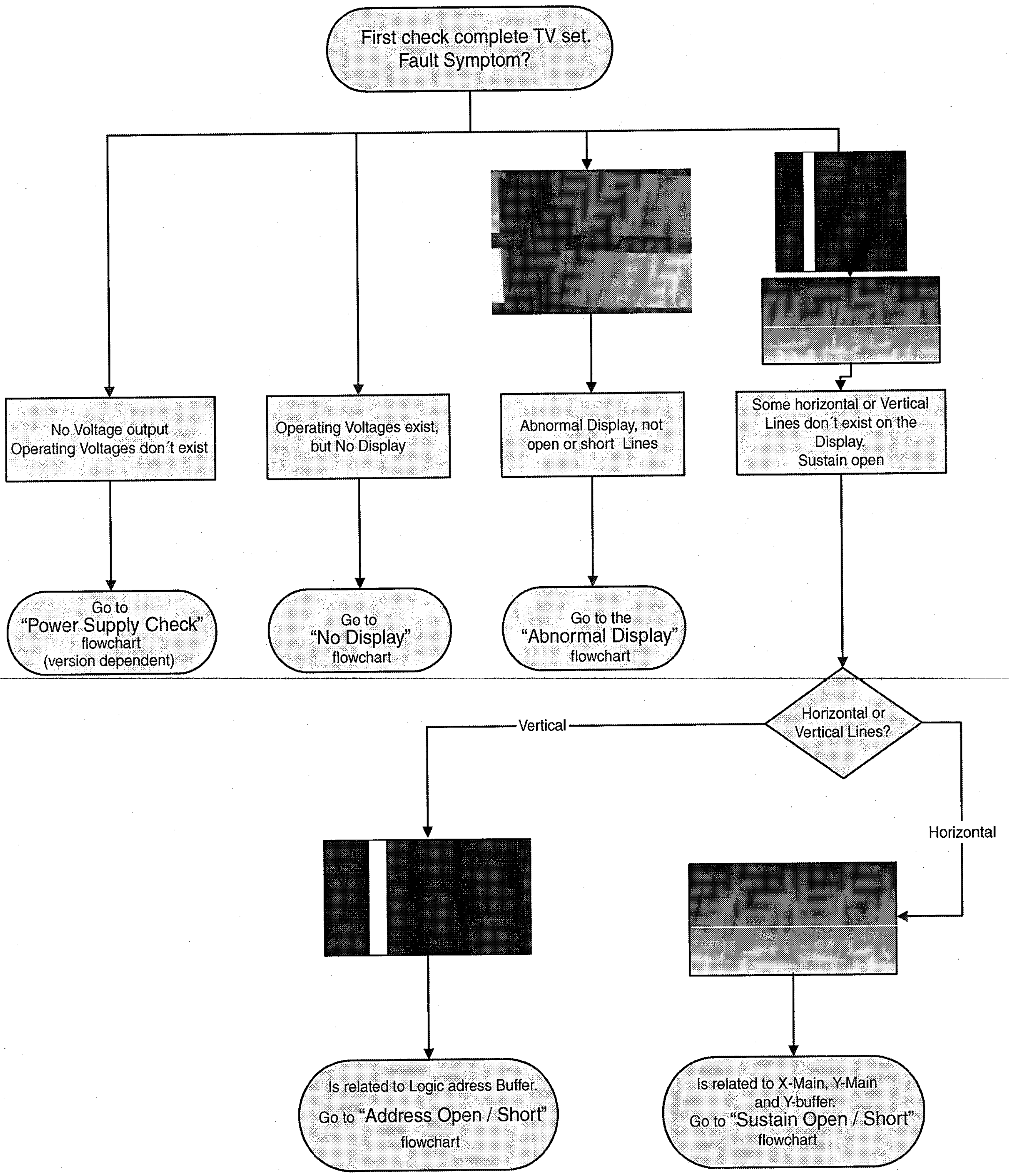

First check complete TV set.
Fault Symptom?
No Voltage output
Operating Voltages don´t exist
Operating Voltages exist, but No Display
Abnormal Display, not open or short Lines
Some horizontal or Vertical Lines don´t exist on the Display.
Sustain open
Go to "Power Supply Check" flowchart (version dependent)
Go to "No Display" flowchart
Go to the "Abnormal Display" flowchart
Horizontal or Vertical Lines?
Vertical
Horizontal
Is related to Logic adress Buffer.
Go to "Address Open / Short" flowchart
Is related to X-Main, Y-Main and Y-buffer.
Go to "Sustain Open / Short" flowchart

Figure 5-5 Fault symptom overview (complete TV set)

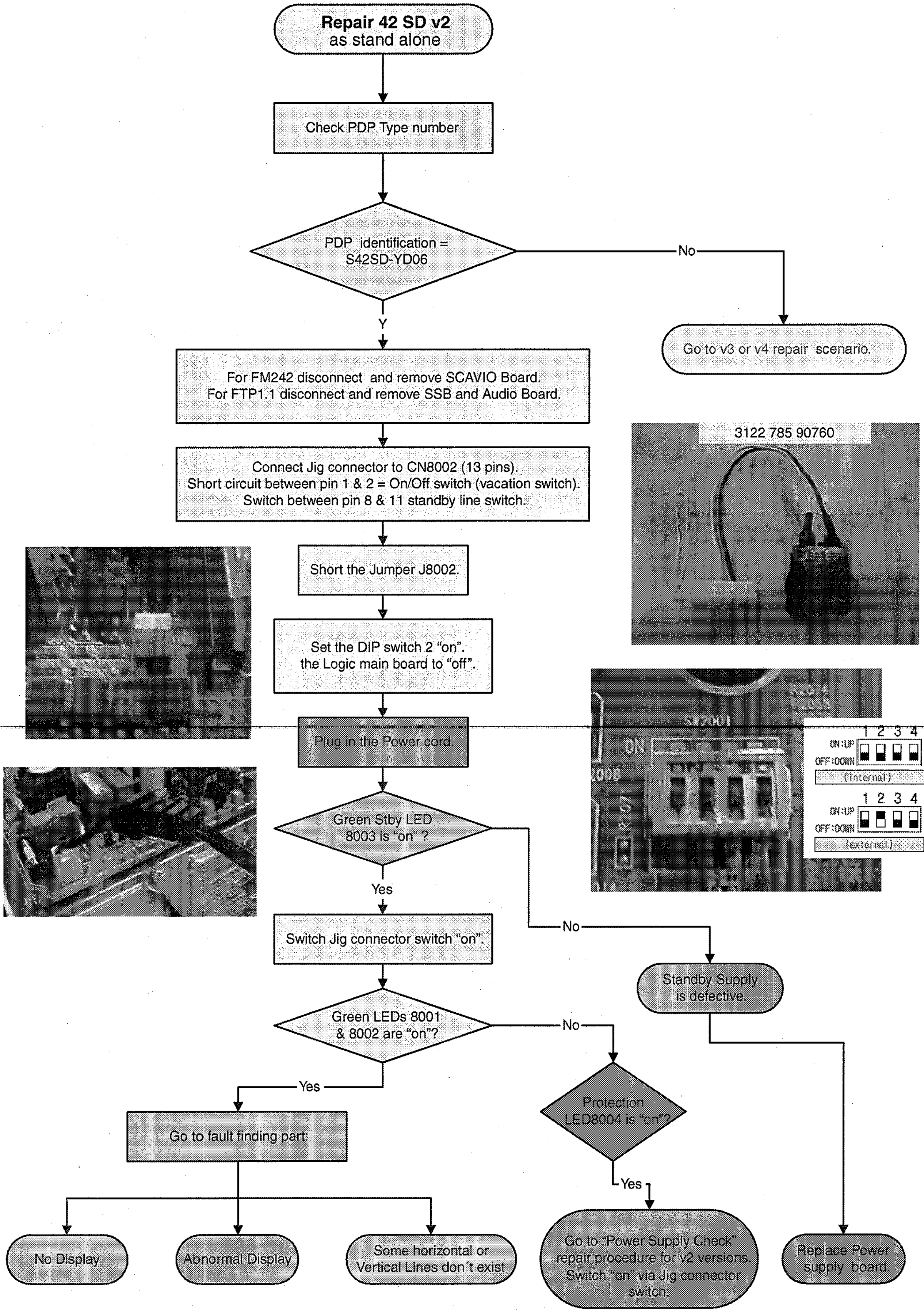

Repair 42 SD v2
as stand alone
Check PDP Type number
PDP identification = S42SD-YD06
No
Go to v3 or v4 repair scenario.
Y
For FM242 disconnect and remove SCAVIO Board.
For FTP1.1 disconnect and remove SSB and Audio Board.
3122 785 90760
Connect Jig connector to CN8002 (13 pins).
Short circuit between pin 1 & 2 = On/Off switch (vacation switch).
Switch between pin 8 & 11 standby line switch.
Short the Jumper J8002.
Set the DIP switch 2 "on".
the Logic main board to "off".
Plug in the Power cord.
SW2001
ON
1 2 3 4
ON:UP
OFF:DOWN
(Internal)
1 2 3 4
ON:UP
OFF:DOWN
(external)
Green Stby LED 8003 is "on" ?
Yes
No
Switch Jig connector switch "on".
Standby Supply is defective.
Green LEDs 8001 & 8002 are "on"?
No
Yes
Protection LED8004 is "on"?
Go to fault finding part
Yes
No Display
Abnormal Display
Some horizontal or Vertical Lines don´t exist
Go to "Power Supply Check" repair procedure for v2 versions. Switch "on" via Jig connector switch.
Replace Power supply board.

Figure 5-6 Repair scenario v2 stand alone panels

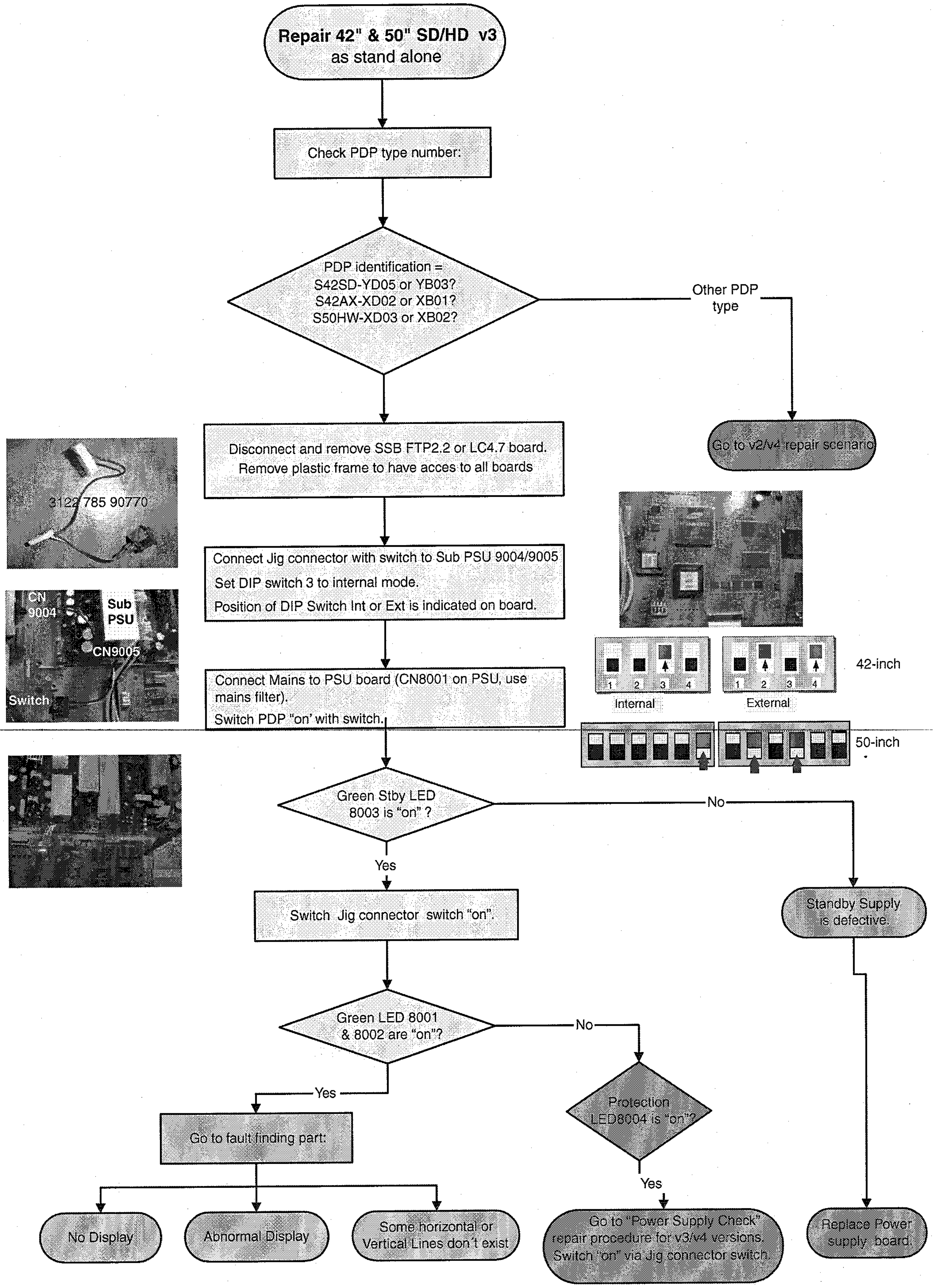
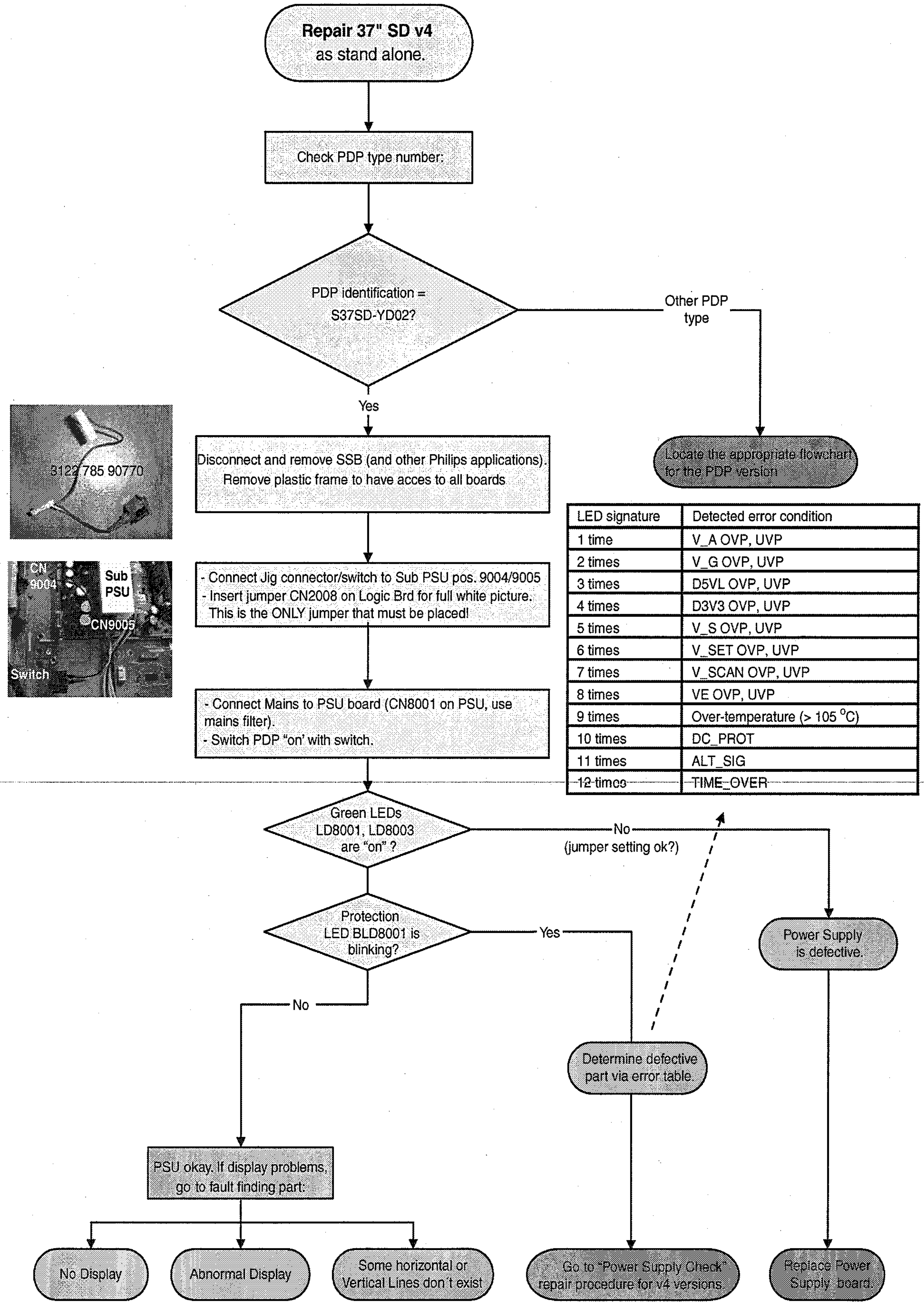

Repair 42" & 50" SD/HD v3
as stand alone
Check PDP type number:
PDP identification =
S42SD-YD05 or YB03?
S42AX-XD02 or XB01?
S50HW-XD03 or XB02?
Other PDP type
Go to v2/v4 repair scenario
Disconnect and remove SSB FTP2.2 or LC4.7 board.
Remove plastic frame to have acces to all boards
3122 785 90770
Connect Jig connector with switch to Sub PSU 9004/9005
Set DIP switch 3 to internal mode.
Position of DIP Switch Int or Ext is indicated on board.
CN 9004
Sub PSU
CN9005
Switch
1 2 3 4
Internal
1 2 3 4
External
42-inch
50-inch
Connect Mains to PSU board (CN8001 on PSU, use mains filter).
Switch PDP "on' with switch.
Green Stby LED 8003 is "on" ?
No
Yes
Standby Supply is defective.
Switch Jig connector switch "on".
Green LED 8001 & 8002 are "on"?
No
Yes
Protection LED8004 is "on"?
Yes
Go to fault finding part:
No Display
Abnormal Display
Some horizontal or Vertical Lines don´t exist
Go to "Power Supply Check" repair procedure for v3/v4 versions. Switch "on" via Jig connector switch.
Replace Power supply board.

Figure 5-7 Repair scenario 42"/50" SD/HD v3 stand alone panels


Repair 37" SD v4 as stand alone.
Check PDP type number:
PDP identification = S37SD-YD02?
Other PDP type
Locate the appropriate flowchart for the PDP version
Yes
3122 785 90770
Disconnect and remove SSB (and other Philips applications). Remove plastic frame to have acces to all boards
CN 9004
Sub PSU
CN9005
Switch
- Connect Jig connector/switch to Sub PSU pos. 9004/9005
- Insert jumper CN2008 on Logic Brd for full white picture. This is the ONLY jumper that must be placed!
- Connect Mains to PSU board (CN8001 on PSU, use mains filter).
- Switch PDP "on' with switch.
Green LEDs LD8001, LD8003 are "on" ?
No (jumper setting ok?)
Power Supply is defective.
Protection LED BLD8001 is blinking?
Yes
No
Determine defective part via error table.
PSU okay. If display problems, go to fault finding part:
No Display
Abnormal Display
Some horizontal or Vertical Lines don't exist
Go to "Power Supply Check" repair procedure for v4 versions.
Replace Power Supply board.
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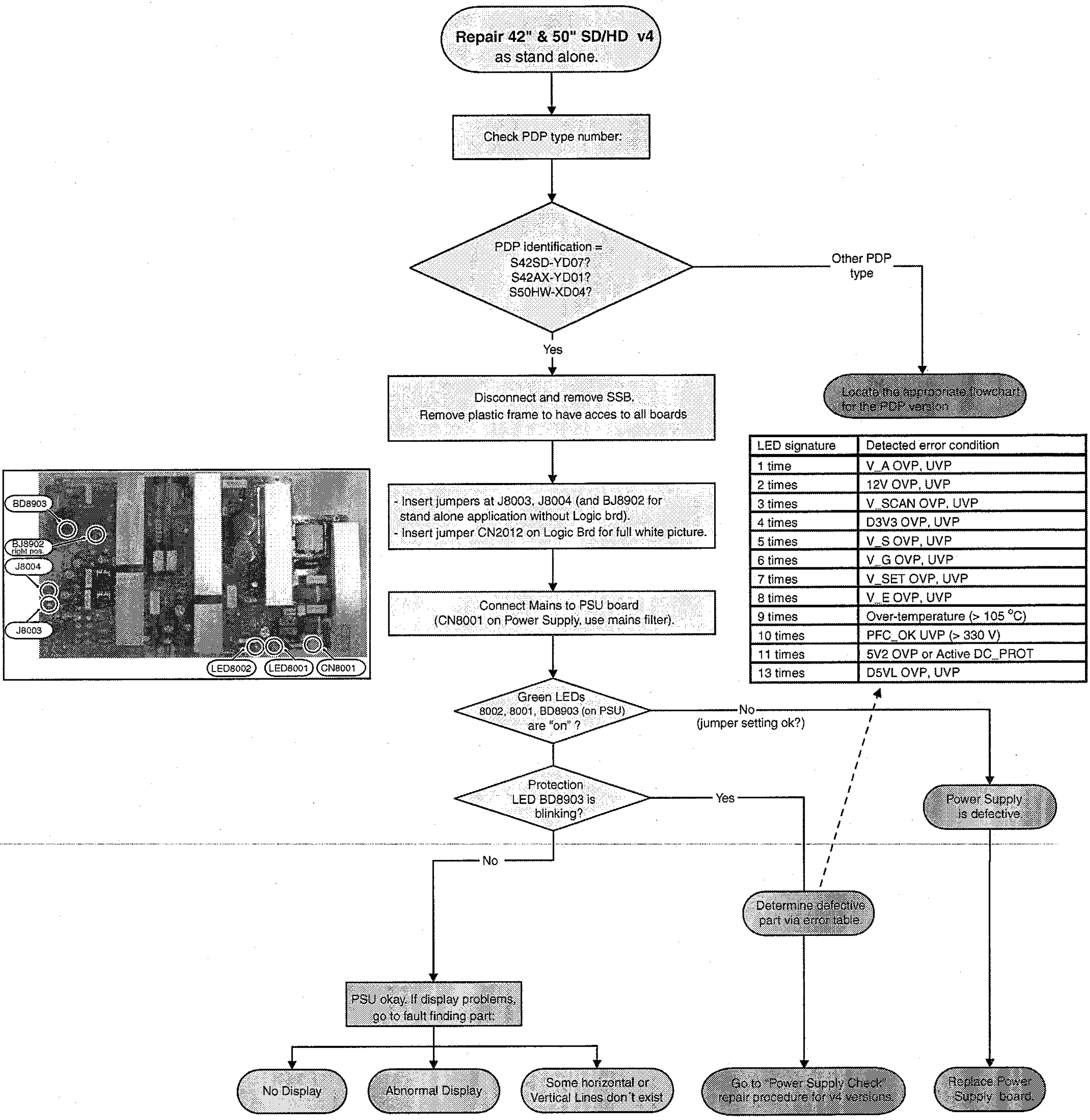
LED signature	Detected error condition
1 time	V_A OVP, UVP
2 times	V_G OVP, UVP
3 times	D5VL OVP, UVP
4 times	D3V3 OVP, UVP
5 times	V_S OVP, UVP
6 times	V_SET OVP, UVP
7 times	V_SCAN OVP, UVP
8 times	VE OVP, UVP
9 times	Over-temperature (> 105 °C)
10 times	DC_PROT
11 times	ALT_SIG
12 times	TIME_OVER

Figure 5-8 Repair scenario 37" SD v4 stand alone panels


Repair 42" & 50" SD/HD v4
as stand alone.
Check PDP type number:
PDP identification =
S42SD-YD07?
S42AX-YD01?
S50HW-XD04?
Other PDP type
Locate the appropriate flowchart for the PDP version
Yes
Disconnect and remove SSB.
Remove plastic frame to have acces to all boards
- Insert jumpers at J8003, J8004 (and BJ8902 for stand alone application without Logic brd).
- Insert jumper CN2012 on Logic Brd for full white picture.
Connect Mains to PSU board
(CN8001 on Power Supply, use mains filter).
BD8903
BJ8902
right pos.
J8004
J8003
LED8002
LED8001
CN8001
Green LEDs
8002, 8001, BD8903 (on PSU)
are "on" ?
No
(jumper setting ok?)
Power Supply is defective.
Protection
LED BD8903 is
blinking?
Yes
No
Determine defective part via error table.
PSU okay. If display problems, go to fault finding part:
No Display
Abnormal Display
Some horizontal or Vertical Lines don't exist
Go to "Power Supply Check" repair procedure for v4 versions.
Replace Power Supply board.
F_14991_037.eps
280306

LED signature	Detected error condition
1 time	V_A OVP, UVP
2 times	12V OVP, UVP
3 times	V_SCAN OVP, UVP
4 times	D3V3 OVP, UVP
5 times	V_S OVP, UVP
6 times	V_G OVP, UVP
7 times	V_SET OVP, UVP
8 times	V_E OVP, UVP
9 times	Over-temperature (> 105 °C)
10 times	PFC_OK UVP (> 330 V)
11 times	5V2 OVP or Active DC_PROT
13 times	D5VL OVP, UVP

Figure 5-9 Repair scenario 42"/50" SD/HD v4 stand alone panels

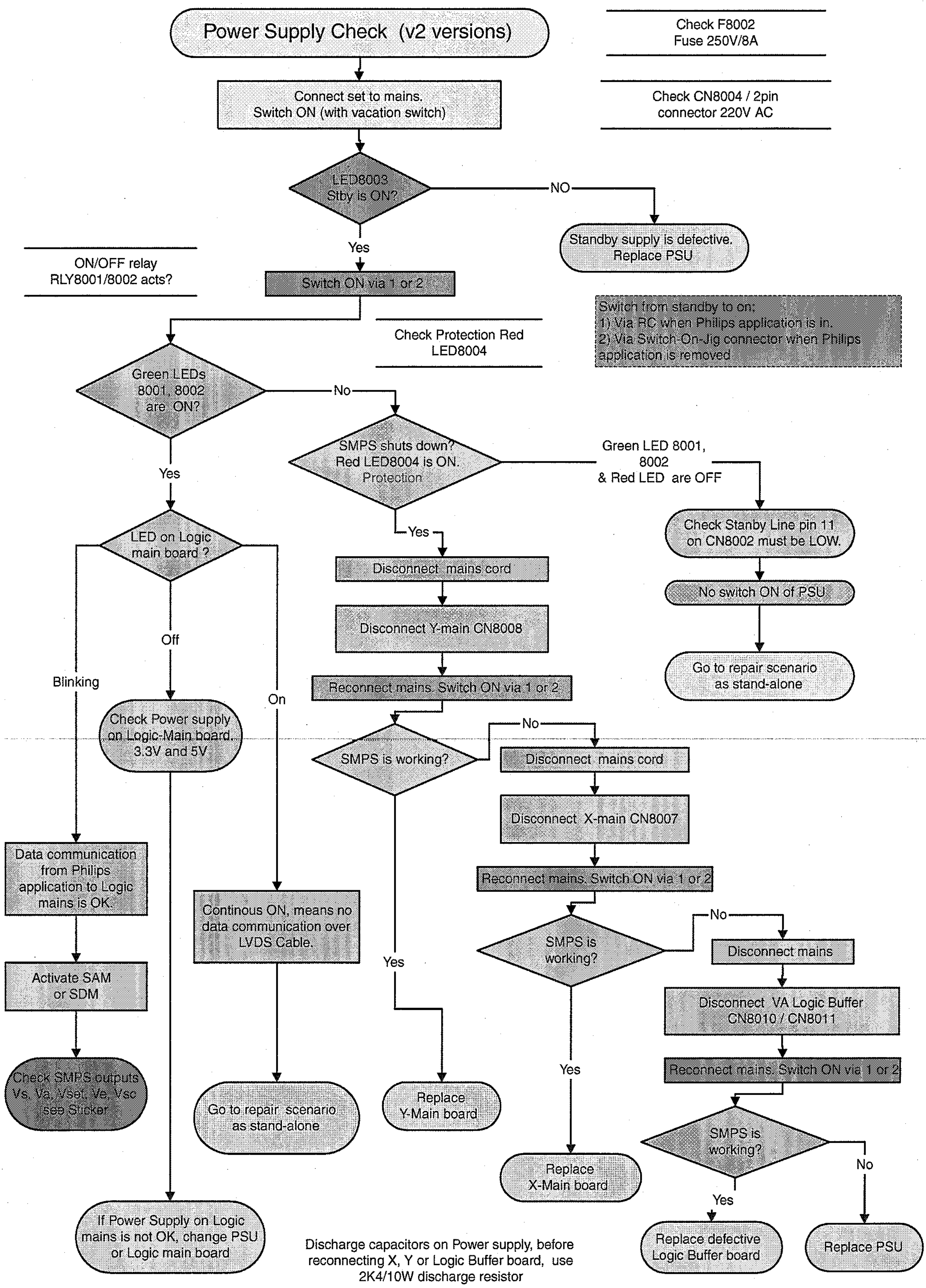

Power Supply Check (v2 versions)
Check F8002 Fuse 250V/8A
Connect set to mains. Switch ON (with vacation switch)
Check CN8004 / 2pin connector 220V AC
LED8003 Stby is ON?
NO
Standby supply is defective. Replace PSU
Yes
ON/OFF relay RLY8001/8002 acts?
Switch ON via 1 or 2
Switch from standby to on: 1) Via RC when Philips application is in. 2) Via Switch-On-Jig connector when Philips application is removed
Check Protection Red LED8004
Green LEDs 8001, 8002 are ON?
No
SMPS shuts down? Red LED8004 is ON. Protection
Green LED 8001, 8002 & Red LED are OFF
Yes
Check Stanby Line pin 11 on CN8002 must be LOW.
No switch ON of PSU
Go to repair scenario as stand-alone
LED on Logic main board ?
Yes
Disconnect mains cord
Disconnect Y-main CN8008
Reconnect mains. Switch ON via 1 or 2
Blinking
Off
On
Check Power supply on Logic-Main board. 3.3V and 5V
No
SMPS is working?
Disconnect mains cord
Disconnect X-main CN8007
Reconnect mains. Switch ON via 1 or 2
Data communication from Philips application to Logic mains is OK.
Continous ON, means no data communication over LVDS Cable.
No
SMPS is working?
Disconnect mains
Yes
Disconnect VA Logic Buffer CN8010 / CN8011
Activate SAM or SDM
Reconnect mains. Switch ON via 1 or 2
Check SMPS outputs Vs, Va, Vset, Ve, Vsc see Sticker
Go to repair scenario as stand-alone
Replace Y-Main board
Yes
SMPS is working?
No
Replace X-Main board
Yes
If Power Supply on Logic mains is not OK, change PSU or Logic main board
Discharge capacitors on Power supply, before reconnecting X, Y or Logic Buffer board, use 2K4/10W discharge resistor
Replace defective Logic Buffer board
Replace PSU

Figure 5-10 Power Supply Check for v2 models

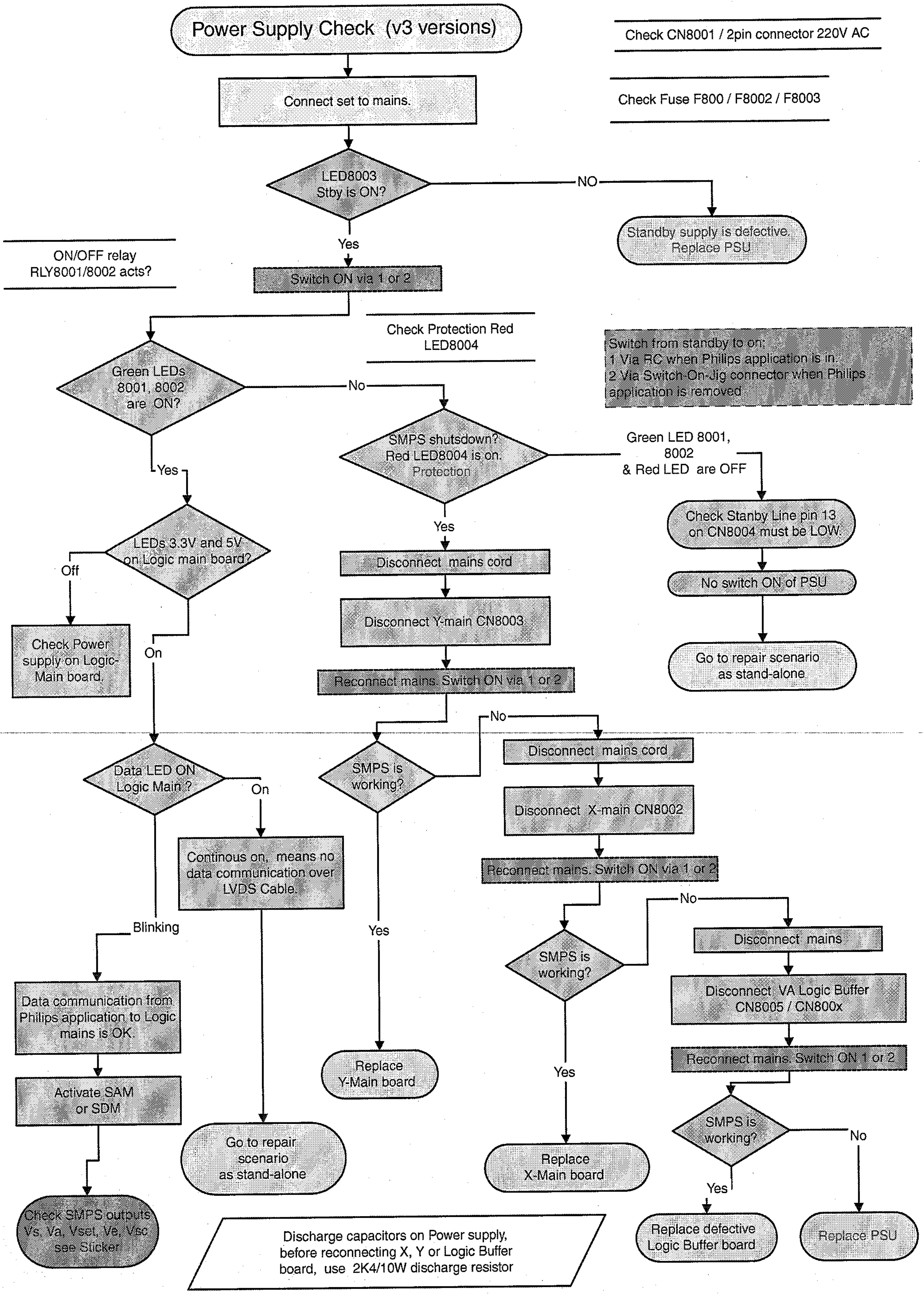

Power Supply Check (v3 versions)
Check CN8001 / 2pin connector 220V AC
Connect set to mains.
Check Fuse F800 / F8002 / F8003
LED8003 Stby is ON?
NO
Standby supply is defective. Replace PSU
Yes
ON/OFF relay RLY8001/8002 acts?
Switch ON via 1 or 2
Check Protection Red LED8004
Switch from standby to on:
1 Via RC when Philips application is in
2 Via Switch On-Jig connector when Philips application is removed
Green LEDs 8001, 8002 are ON?
No
SMPS shutsdown? Red LED8004 is on. Protection
Green LED 8001, 8002 & Red LED are OFF
Check Stanby Line pin 13 on CN8004 must be LOW
No switch ON of PSU
Go to repair scenario as stand-alone
Yes
LEDs 3.3V and 5V on Logic main board?
Off
Check Power supply on Logic-Main board.
On
Yes
Disconnect mains cord
Disconnect Y-main CN8003
Reconnect mains. Switch ON via 1 or 2
No
Data LED ON Logic Main ?
On
Continous on, means no data communication over LVDS Cable.
SMPS is working?
Disconnect mains cord
Disconnect X-main CN8002
Reconnect mains. Switch ON via 1 or 2
Blinking
Yes
No
Data communication from Philips application to Logic mains is OK.
SMPS is working?
Disconnect mains
Disconnect VA Logic Buffer CN8005 / CN800x
Activate SAM or SDM
Replace Y-Main board
Yes
Reconnect mains. Switch ON 1 or 2
SMPS is working?
No
Go to repair scenario as stand-alone
Replace X-Main board
Yes
Check SMPS outputs Vs, Va, Vset, Ve, Vsc see Sticker
Discharge capacitors on Power supply, before reconnecting X, Y or Logic Buffer board, use 2K4/10W discharge resistor
Replace defective Logic Buffer board
Replace PSU

Figure 5-11 Power Supply Check for v3 models

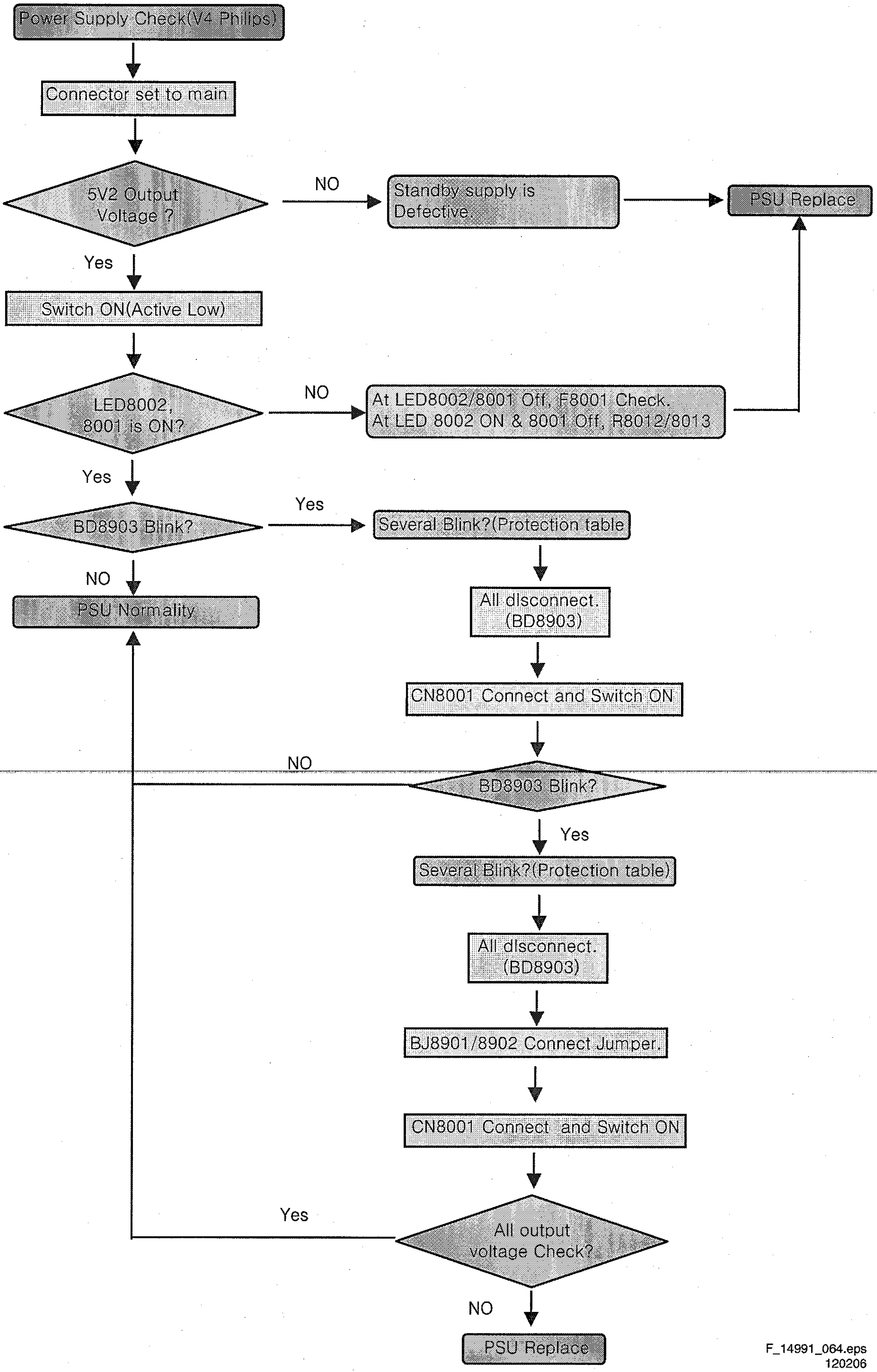

Power Supply Check(V4 Philips)
Connector set to main
5V2 Output Voltage ?
NO
Standby supply is Defective.
PSU Replace
Yes
Switch ON(Active Low)
LED8002, 8001 is ON?
NO
At LED8002/8001 Off, F8001 Check.
At LED 8002 ON & 8001 Off, R8012/8013
Yes
BD8903 Blink?
Yes
Several Blink?(Protection table
NO
PSU Normality
All disconnect. (BD8903)
CN8001 Connect and Switch ON
NO
BD8903 Blink?
Yes
Several Blink?(Protection table)
All disconnect. (BD8903)
BJ8901/8902 Connect Jumper.
CN8001 Connect and Switch ON
Yes
All output voltage Check?
NO
PSU Replace

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Figure 5-12 Power Supply Check for v4 models

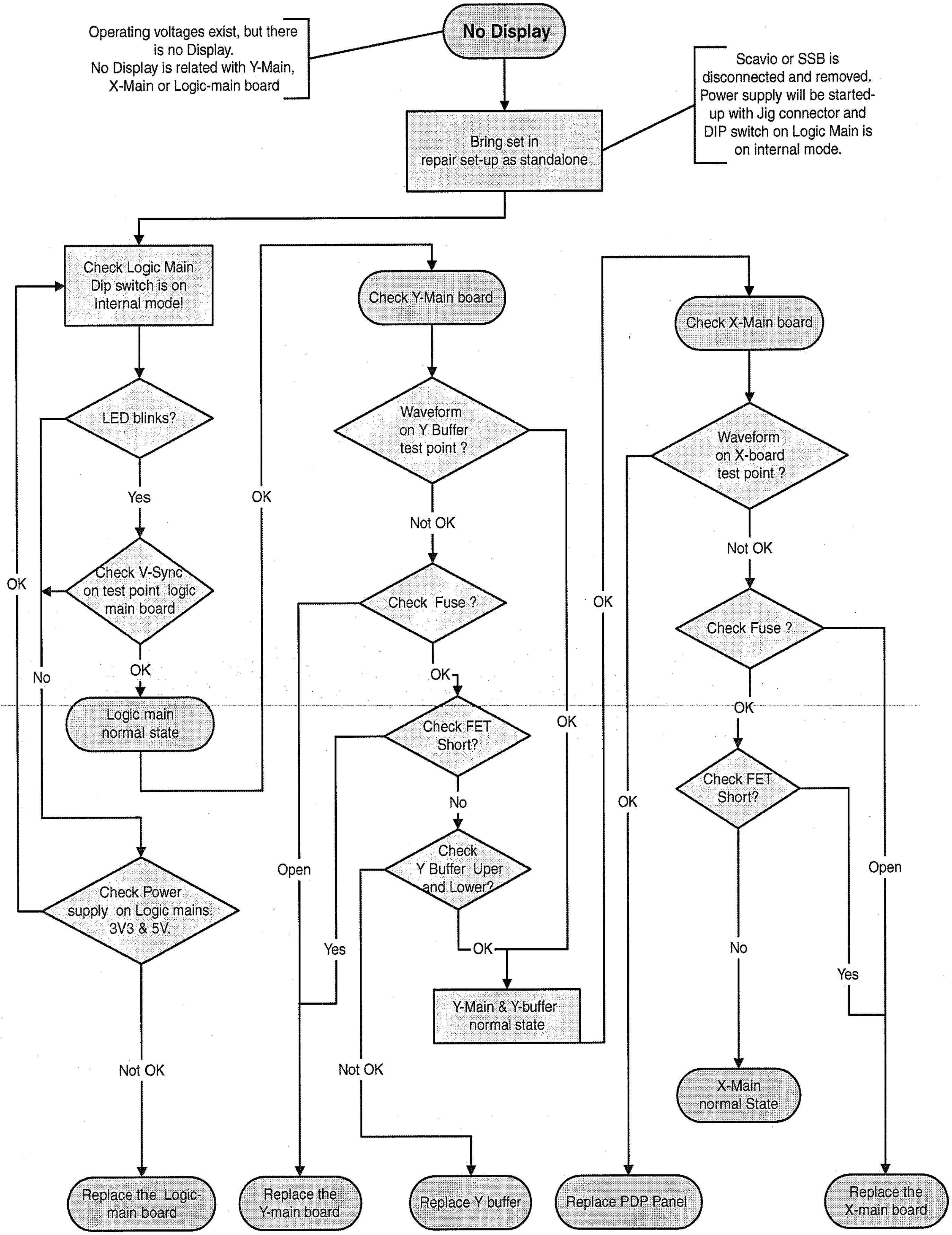

No Display
Operating voltages exist, but there is no Display. No Display is related with Y-Main, X-Main or Logic-main board
Bring set in repair set-up as standalone
Scavio or SSB is disconnected and removed. Power supply will be started-up with Jig connector and DIP switch on Logic Main is on internal mode.
Check Logic Main Dip switch is on Internal mode!
LED blinks?
Yes
No
Check V-Sync on test point logic main board
OK
OK
Logic main normal state
OK
Check Power supply on Logic mains. 3V3 & 5V.
Not OK
Replace the Logic-main board
Check Y-Main board
Waveform on Y Buffer test point ?
Not OK
Check Fuse ?
Open
OK
Check FET Short?
Yes
No
Check Y Buffer Uper and Lower?
Not OK
OK
OK
Y-Main & Y-buffer normal state
Replace the Y-main board
Replace Y buffer
OK
Check X-Main board
Waveform on X-board test point ?
OK
Not OK
Check Fuse ?
OK
Open
Check FET Short?
No
Yes
X-Main normal State
Replace PDP Panel
Replace the X-main board

Figure 5-13 Fault symptom: "No Display"

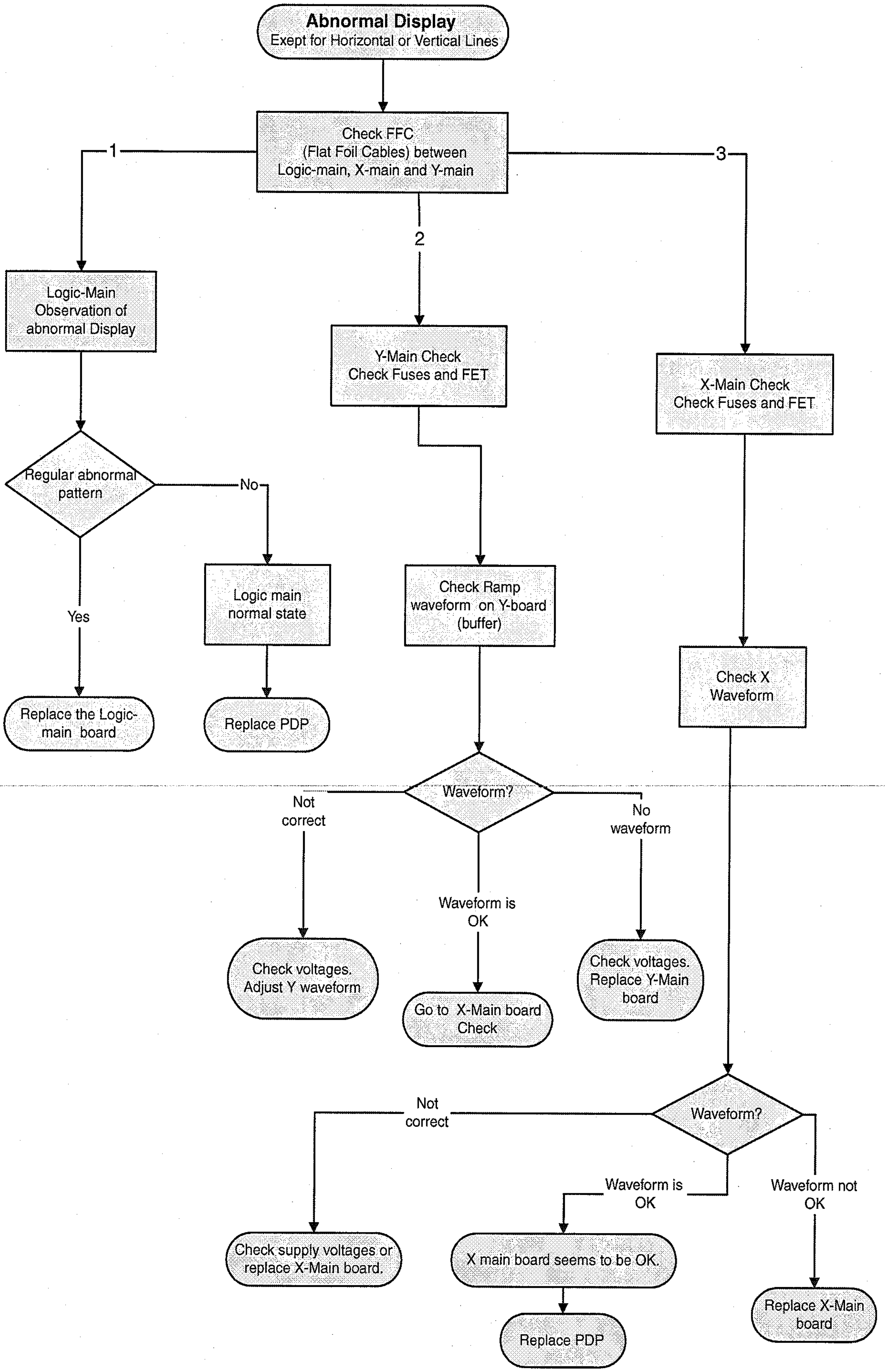

Abnormal Display
Exept for Horizontal or Vertical Lines
Check FFC
(Flat Foil Cables) between
Logic-main, X-main and Y-main
1
2
3
Logic-Main
Observation of
abnormal Display
Regular abnormal
pattern
No
Yes
Logic main
normal state
Replace the Logic-
main board
Replace PDP
Y-Main Check
Check Fuses and FET
Check Ramp
waveform on Y-board
(buffer)
Waveform?
Not
correct
No
waveform
Waveform is
OK
Check voltages.
Adjust Y waveform
Go to X-Main board
Check
Check voltages.
Replace Y-Main
board
X-Main Check
Check Fuses and FET
Check X
Waveform
Waveform?
Not
correct
Waveform is
OK
Waveform not
OK
Check supply voltages or
replace X-Main board.
X main board seems to be OK.
Replace PDP
Replace X-Main
board

Figure 5-14 Fault symptom: "Abnormal Display"

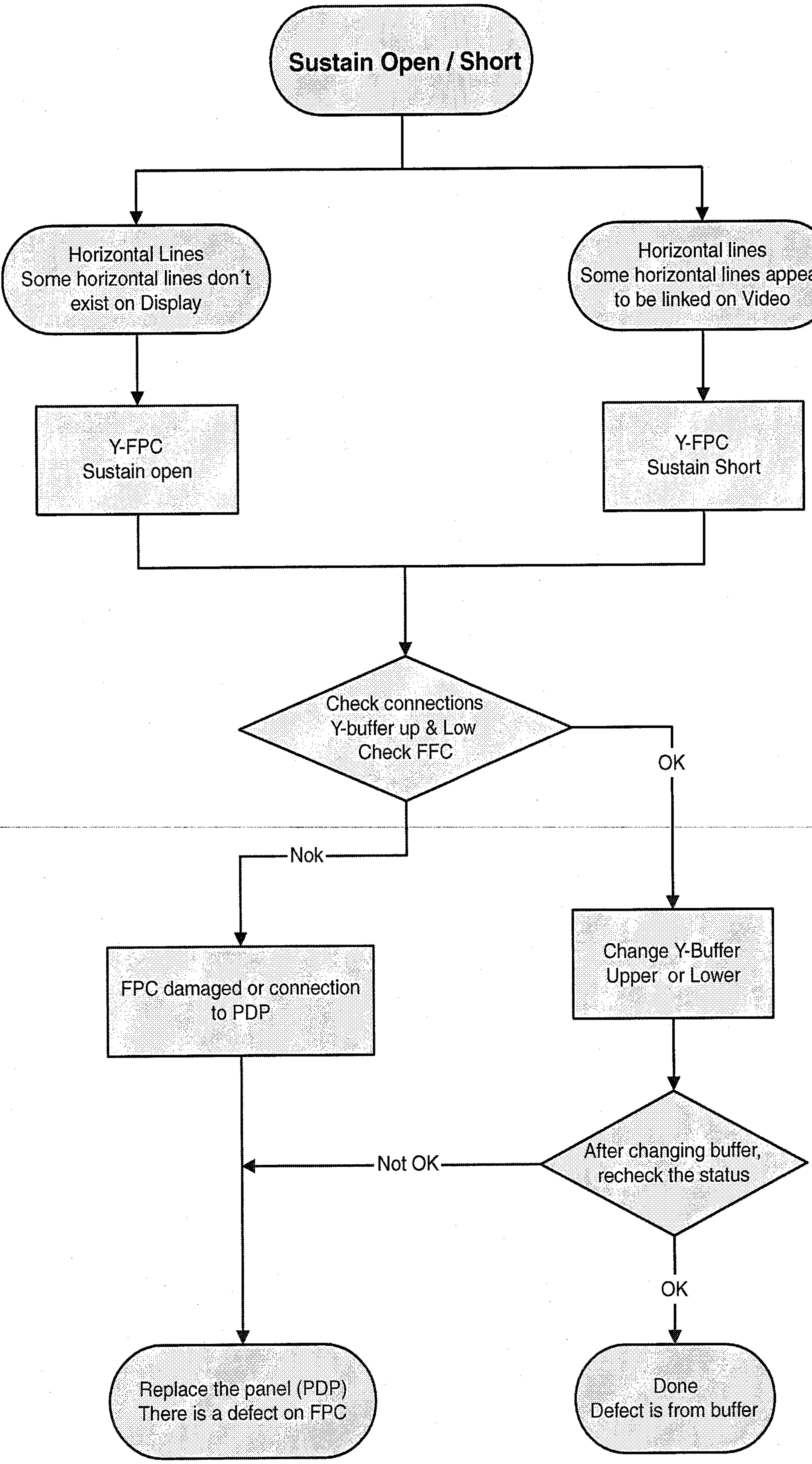

Sustain Open / Short
Horizontal Lines
Some horizontal lines don´t exist on Display
Horizontal lines
Some horizontal lines appear to be linked on Video
Y-FPC
Sustain open
Y-FPC
Sustain Short
Check connections
Y-buffer up & Low
Check FFC
OK
Nok
FPC damaged or connection to PDP
Change Y-Buffer
Upper or Lower
After changing buffer, recheck the status
Not OK
OK
Replace the panel (PDP)
There is a defect on FPC
Done
Defect is from buffer

Figure 5-15 Fault symptom: "Sustain open / short"

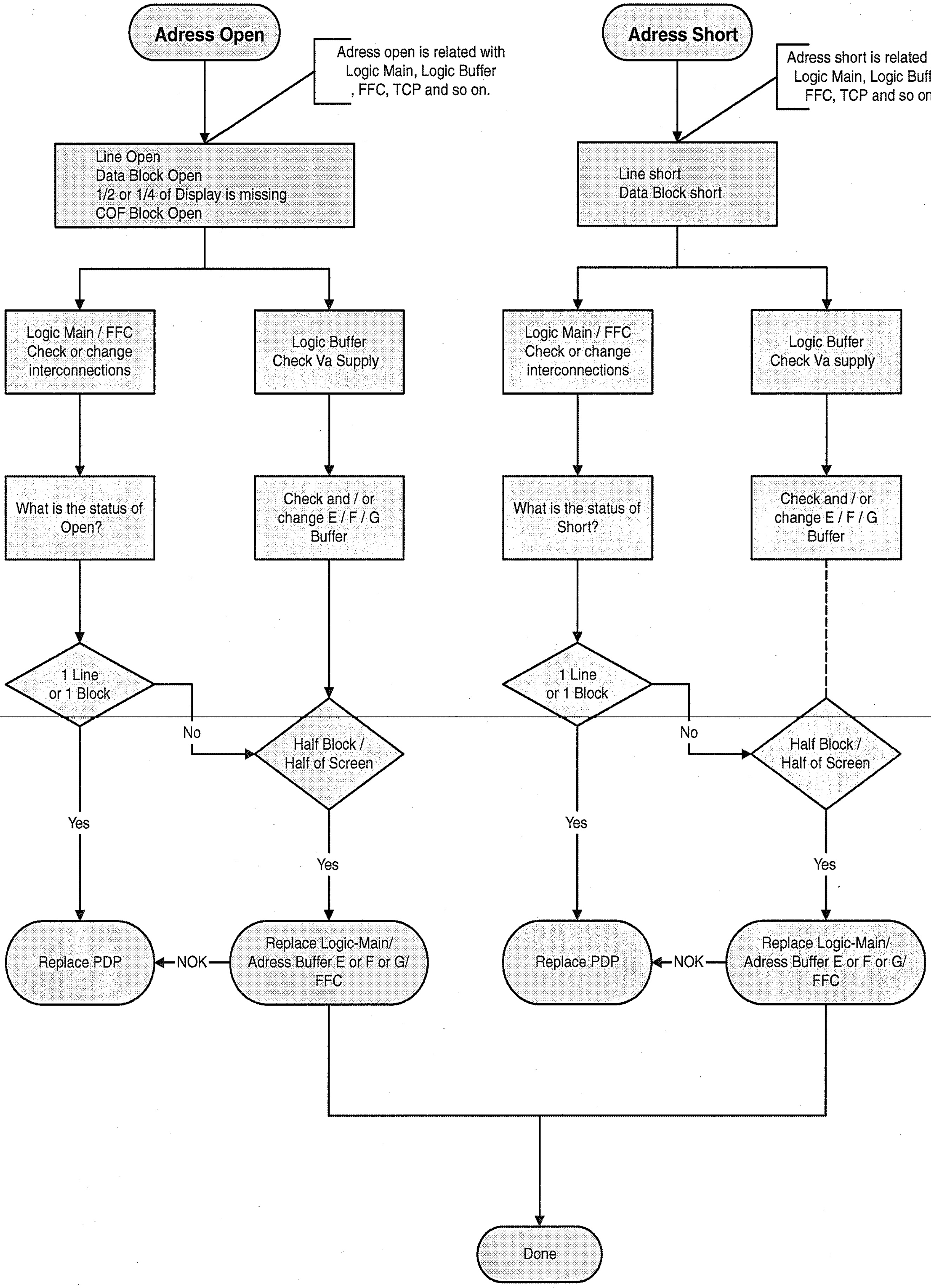
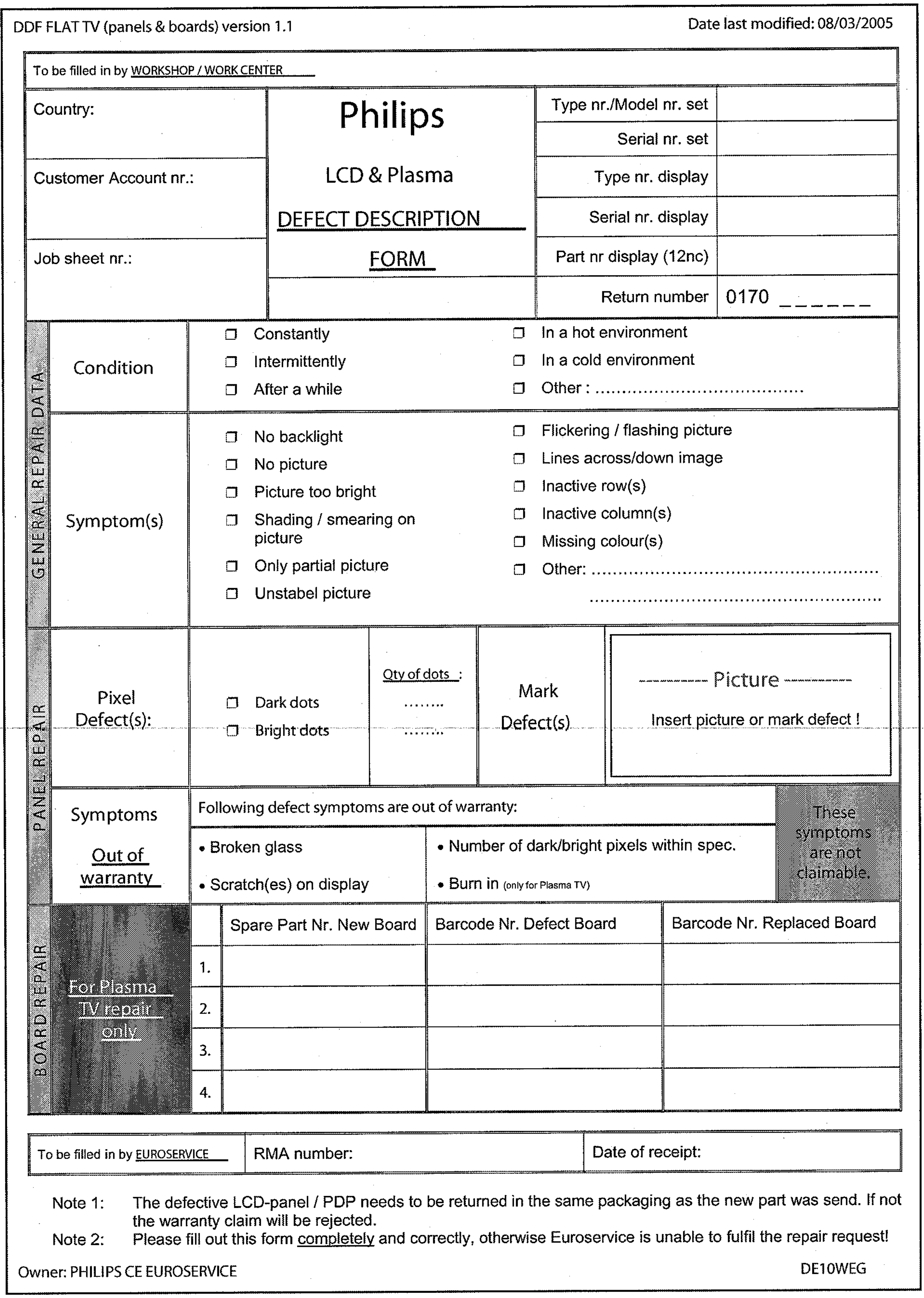

Adress Open
Adress open is related with Logic Main, Logic Buffer , FFC, TCP and so on.
Line Open
Data Block Open
1/2 or 1/4 of Display is missing
COF Block Open
Logic Main / FFC Check or change interconnections
Logic Buffer Check Va Supply
What is the status of Open?
Check and / or change E / F / G Buffer
1 Line or 1 Block
No
Half Block / Half of Screen
Yes
Yes
Replace PDP
NOK
Replace Logic-Main/ Adress Buffer E or F or G/ FFC
Adress Short
Adress short is related with Logic Main, Logic Buffer, FFC, TCP and so on.
Line short
Data Block short
Logic Main / FFC Check or change interconnections
Logic Buffer Check Va supply
What is the status of Short?
Check and / or change E / F / G Buffer
1 Line or 1 Block
No
Half Block / Half of Screen
Yes
Yes
Replace PDP
NOK
Replace Logic-Main/ Adress Buffer E or F or G/ FFC
Done

Figure 5-16 Fault symptom: "Address open / short"

5.3 Defect Description Form

This form must be used by the workshops for warranty claims:



DDF FLAT TV (panels & boards) version 1.1

Date last modified: 08/03/2005

To be filled in by WORKSHOP / WORK CENTER

Country:	Philips LCD & Plasma DEFECT DESCRIPTION FORM	Type nr./Model nr. set	
		Serial nr. set	
Customer Account nr.:		Type nr. display	
		Serial nr. display	
Job sheet nr.:		Part nr display (12nc)	
		Return number	0170 ______

GENERAL REPAIR DATA	Condition	☐ Constantly ☐ Intermittently ☐ After a while	☐ In a hot environment ☐ In a cold environment ☐ Other : ....
	Symptom(s)	☐ No backlight ☐ No picture ☐ Picture too bright ☐ Shading / smearing on picture ☐ Only partial picture ☐ Unstabel picture	☐ Flickering / flashing picture ☐ Lines across/down image ☐ Inactive row(s) ☐ Inactive column(s) ☐ Missing colour(s) ☐ Other: ....

PANEL REPAIR	Pixel Defect(s):	☐ Dark dots ☐ Bright dots	Qty of dots :	Mark Defect(s)	---------- Picture ---------- Insert picture or mark defect !

PANEL REPAIR	Symptoms Out of warranty	Following defect symptoms are out of warranty: • Broken glass • Scratch(es) on display	• Number of dark/bright pixels within spec. • Burn in (only for Plasma TV)	These symptoms are not claimable.

BOARD REPAIR		Spare Part Nr. New Board	Barcode Nr. Defect Board	Barcode Nr. Replaced Board
For Plasma TV repair only	1.			
	2.			
	3.			
	4.			

To be filled in by EUROSERVICE	RMA number:	Date of receipt:

Note 1: The defective LCD-panel / PDP needs to be returned in the same packaging as the new part was send. If not the warranty claim will be rejected.

Note 2: Please fill out this form completely and correctly, otherwise Euroservice is unable to fulfil the repair request!

Owner: PHILIPS CE EUROSERVICE

DE10WEG

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110705

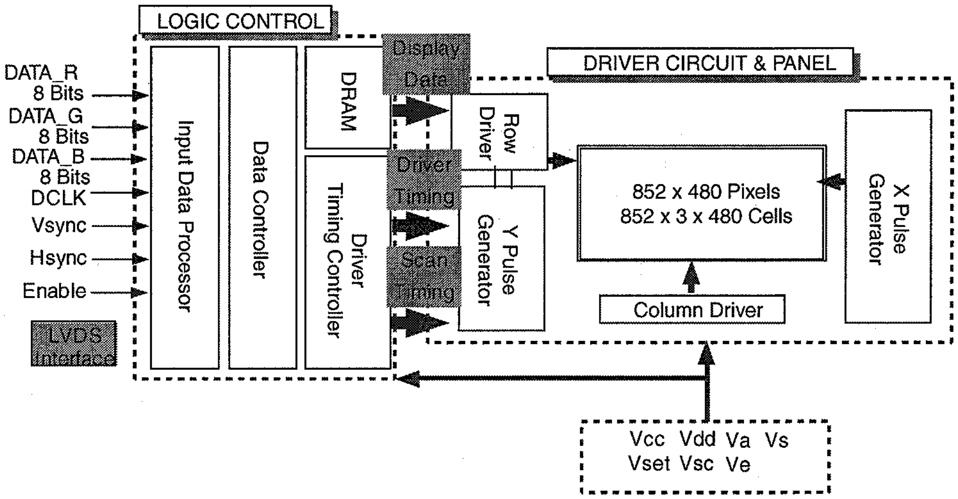
Figure 5-17 Defect Description Form (DDF)

6. Block Diagrams, Test Point Overview, and Waveforms

Index of this chapter:

6.1 Block Diagram for Logic Circuit
6.2 PSU Board diagram

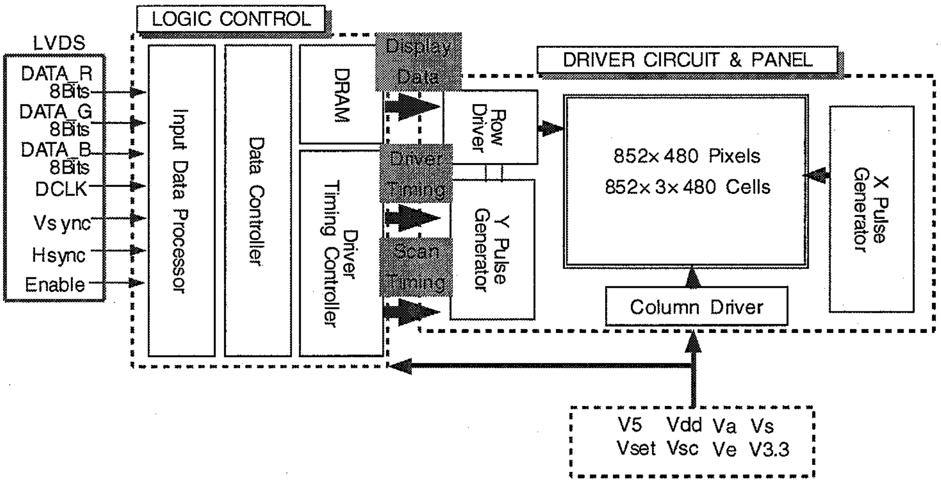
6.1 Block Diagram for Logic Circuit


LOGIC CONTROL
DATA_R
8 Bits
DATA_G
8 Bits
DATA_B
8 Bits
DCLK
Vsync
Hsync
Enable
LVDS Interface
Input Data Processor
Data Controller
DRAM
Driver Timing Controller
Display Data
Driver Timing
Scan Timing
DRIVER CIRCUIT & PANEL
Row Driver
Y Pulse Generator
852 x 480 Pixels
852 x 3 x 480 Cells
Column Driver
X Pulse Generator
Vcc Vdd Va Vs
Vset Vsc Ve

Reference

- Vcc : Voltage for Logic Control
- Vdd : Voltage for FET driver
- Va : Voltage for address pulse
- Vs : Voltage sustain pulse
- Vsc : Voltage for scan pulse
- Ve : Voltage for X ramp pulse
- Vset : Voltage for Y ramp pulse

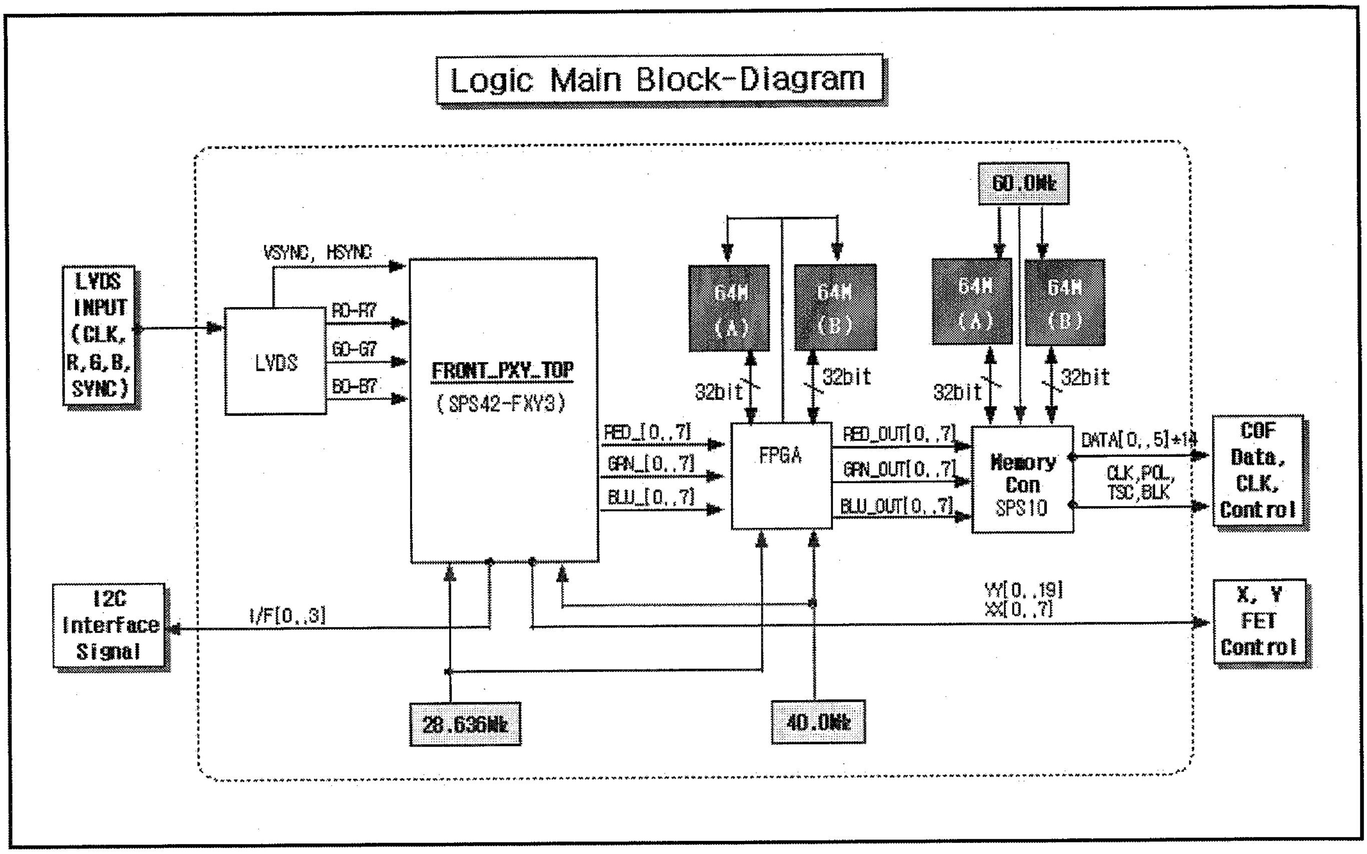
Figure 6-1 Block diagram (37" SD v4)


LOGIC CONTROL
LVDS
DATA_R
8Bits
DATA_G
8Bits
DATA_B
8Bits
DCLK
Vs ync
Hsync
Enable
Input Data Processor
Data Controller
DRAM
Driver Timing Controller
Display Data
Driver Timing
Scan Timing
DRIVER CIRCUIT & PANEL
Row Driver
Y Pulse Generator
852× 480 Pixels
852× 3× 480 Cells
Column Driver
X Pulse Generator
V5 Vdd Va Vs
Vset Vsc Ve V3.3

Reference

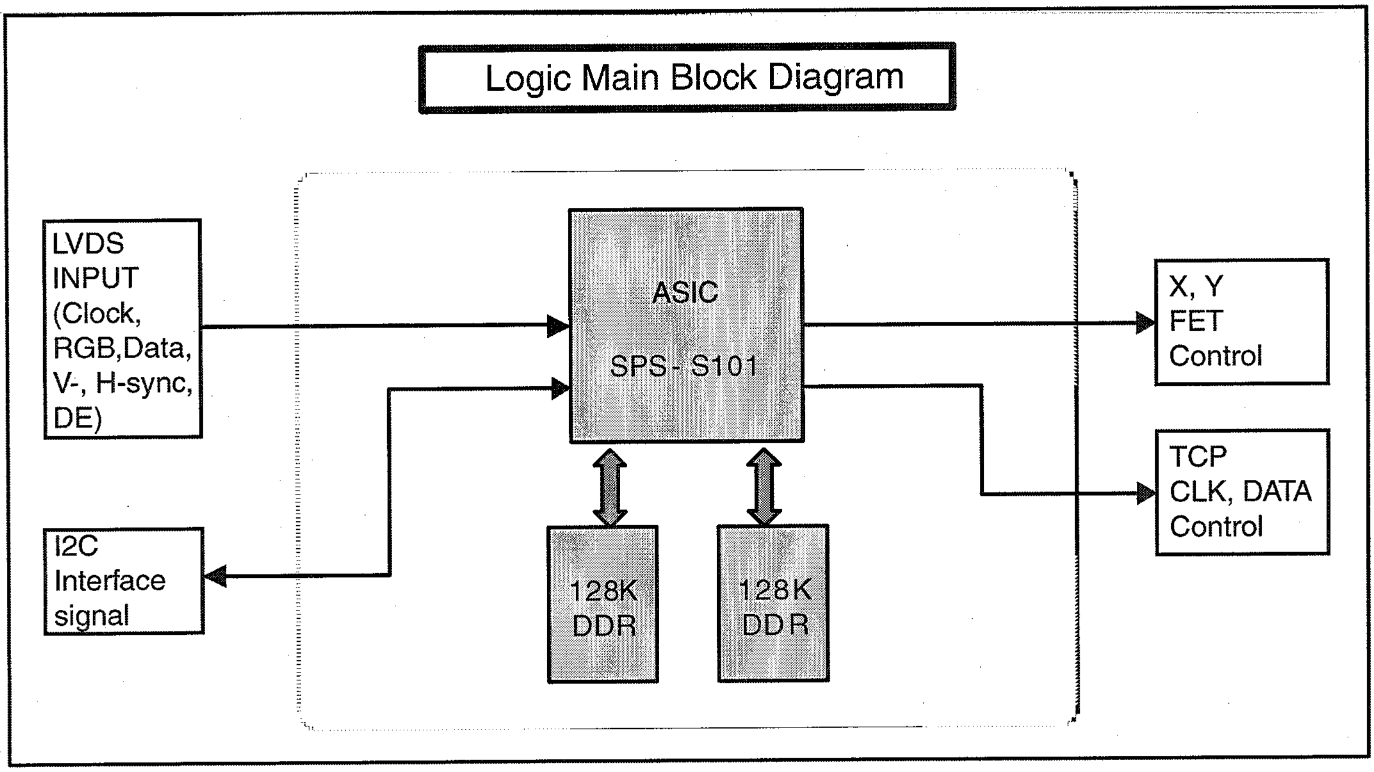
-V3.3 : Voltage for LOGIC Control
-V5 : Voltage for COF driver
-Vdd : Voltage for FET driver
-Va : Voltage for address pulse
-Vs : Voltage for sustain driver
-Vsc : Voltage for scan pulse
-Ve : Voltage for X ramppulse
-Vset : Voltage for Y ramppulse

Figure 6-2 Block diagram (42" SD v2)


Logic Main Block-Diagram
LVDS INPUT (CLK, R,G,B, SYNC)
LVDS
VSYNC, HSYNC
R0-R7
G0-G7
B0-B7
FRONT_PXY_TOP
(SPS42-FXY3)
RED_[0..7]
GRN_[0..7]
BLU_[0..7]
64M (A)
64M (B)
32bit
32bit
FPGA
RED_OUT[0..7]
GRN_OUT[0..7]
BLU_OUT[0..7]
60.0㎒
64M (A)
64M (B)
32bit
32bit
Memory Con SPS10
DATA[0..5]*14
CLK,POL, TSC,BLK
COF Data, CLK, Control
I2C Interface Signal
I/F[0..3]
YY[0..19]
XX[0..7]
X, Y FET Control
28.636㎒
40.0㎒

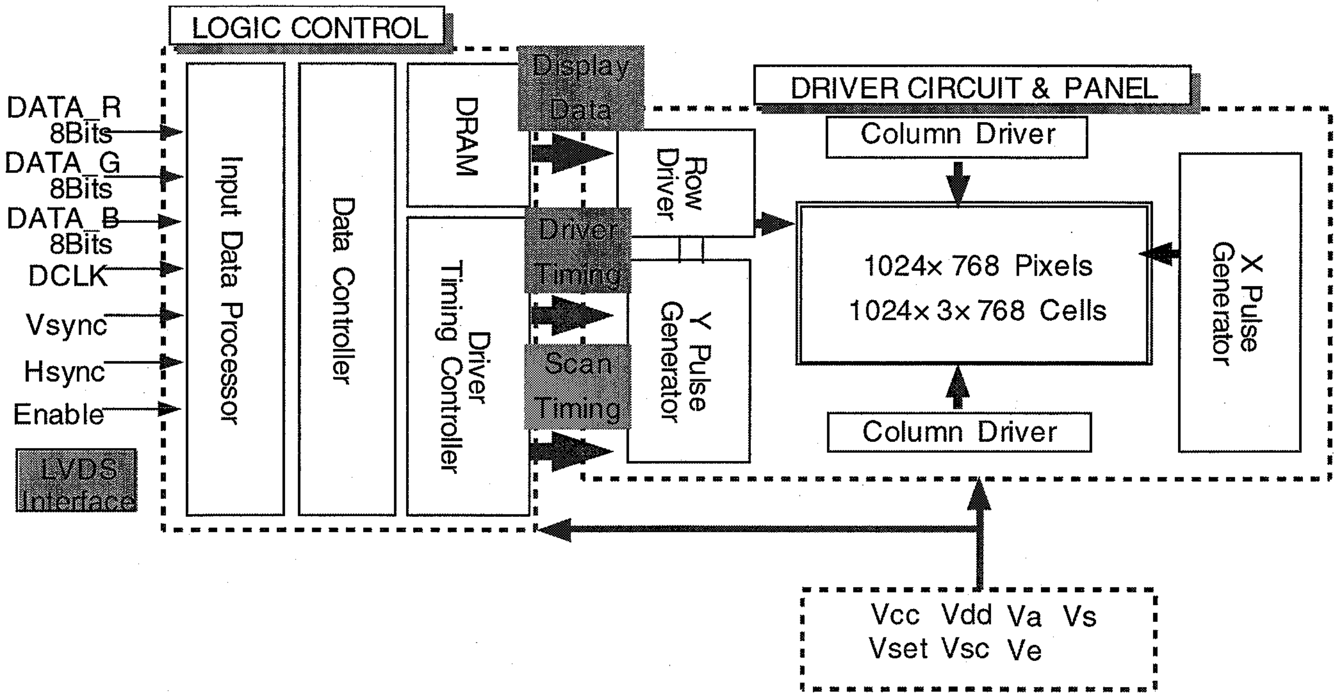
F_14991_032.eps
030805

Figure 6-3 Block diagram (42" SD v3)


Logic Main Block Diagram
LVDS INPUT (Clock, RGB,Data, V-, H-sync, DE)
I2C Interface signal
ASIC
SPS - S101
128K DDR
128K DDR
X, Y FET Control
TCP CLK, DATA Control

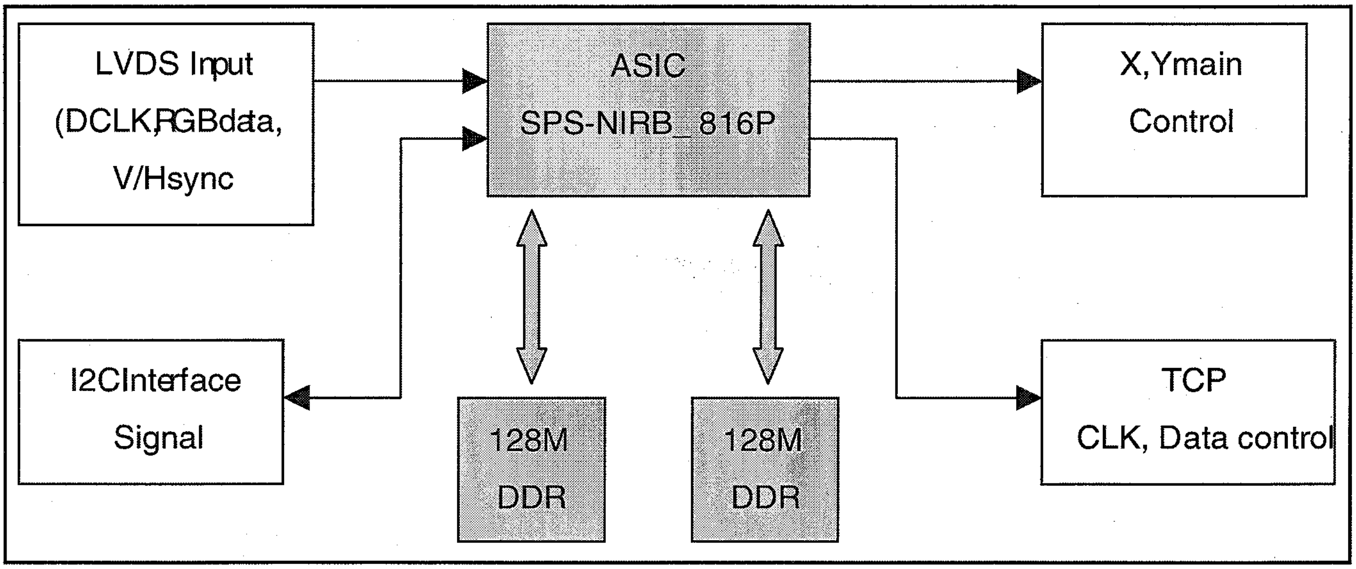
F_14991_002.eps
180705

Figure 6-4 Block diagram (42" SD v4)


LOGIC CONTROL
DATA_R
8Bits
DATA_G
8Bits
DATA_B
8Bits
DCLK
Vsync
Hsync
Enable
LVDS Interface
Input Data Processor
Data Controller
DRAM
Driver Timing Controller
Display Data
Driver Timing
Scan Timing
DRIVER CIRCUIT & PANEL
Row Driver
Y Pulse Generator
Column Driver
1024x 768 Pixels
1024x 3x 768 Cells
Column Driver
X Pulse Generator
Vcc Vdd Va Vs
Vset Vsc Ve

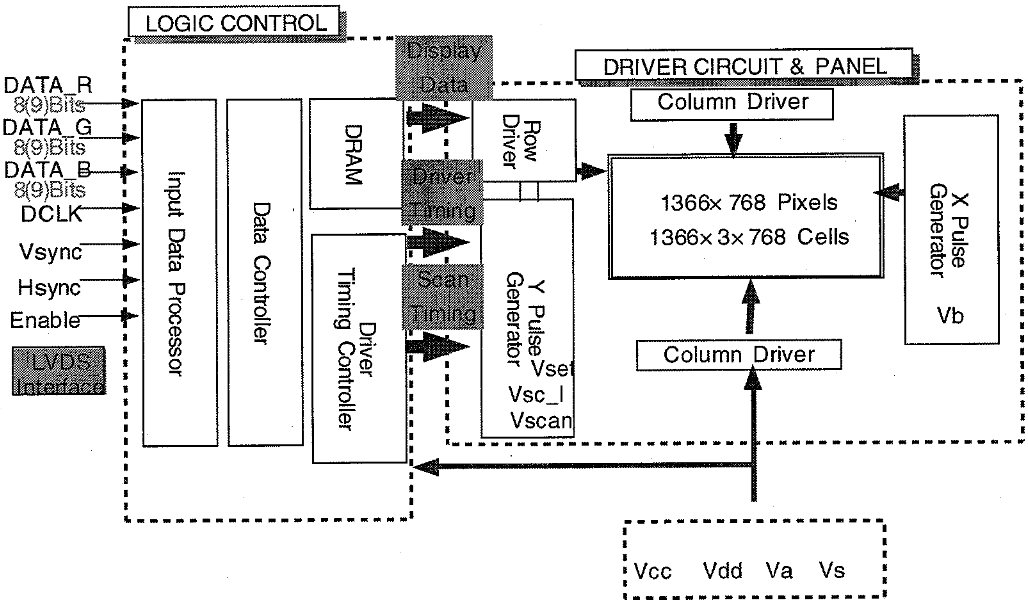
Reference
- Vcc : Voltage for Logic Control
- Vdd : Voltage for Fet driver
- Va : Voltage for address pulse
- Vs : Voltage sustain pulse
- Vsc : Voltage for scan pulse
- Ve : Voltage for X ramp pulse
- Vset : Voltage for Y ramp pulse

Figure 6-5 Block diagram (42" HD v3)


LVDS Input
(DCLK,RGBdata,
V/Hsync
ASIC
SPS-NIRB_816P
X,Ymain
Control
I2CInterface
Signal
128M
DDR
128M
DDR
TCP
CLK, Data control

F_14991_018.eps
030805

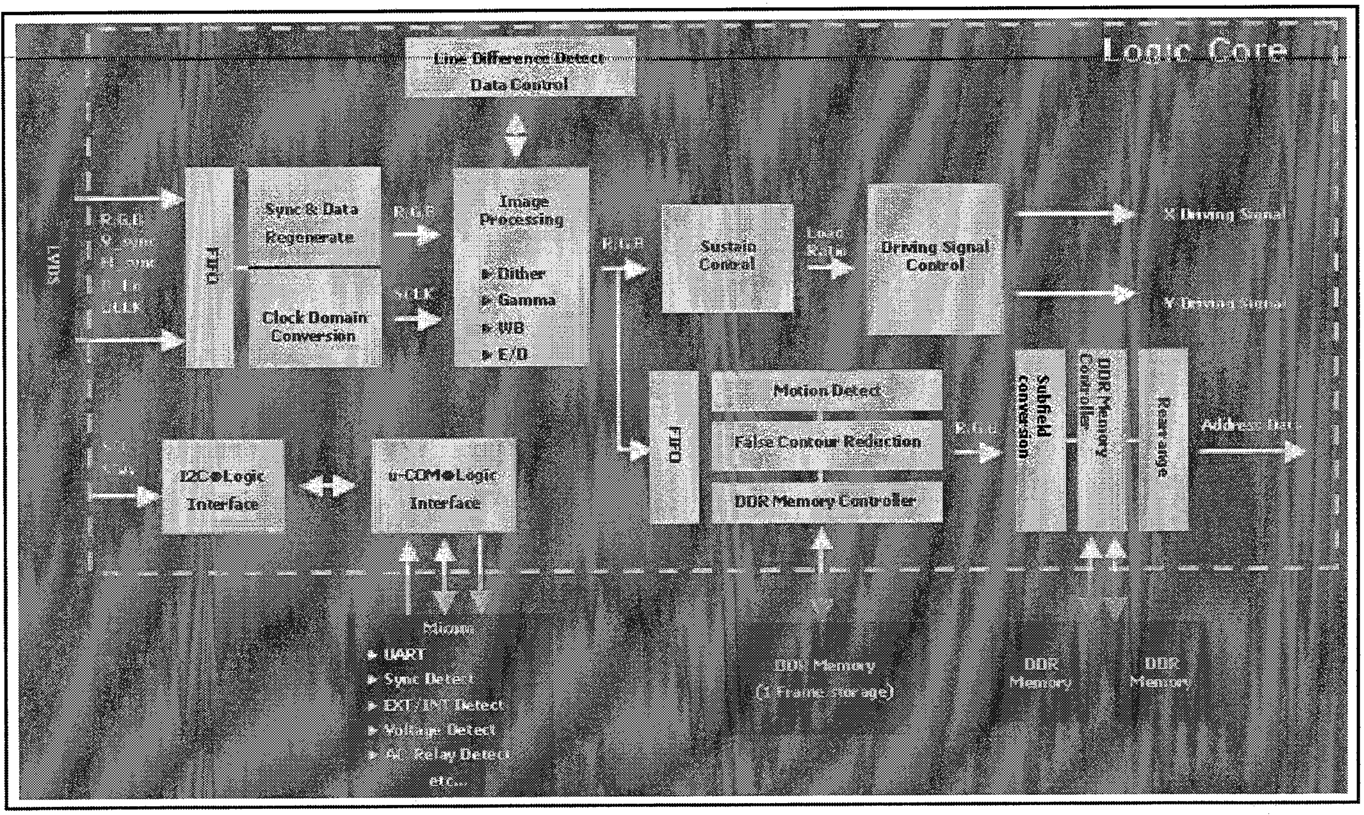
Figure 6-6 Block diagram (42" HD v4)


LOGIC CONTROL
DATA_R
8(9)Bits
DATA_G
8(9)Bits
DATA_B
8(9)Bits
DCLK
Vsync
Hsync
Enable
LVDS Interface
Input Data Processor
Data Controller
DRAM
Driver Timing Controller
Display Data
Driver Timing
Scan Timing
Row Driver
Y Pulse Generator
Vset
Vsc_l
Vscan
DRIVER CIRCUIT & PANEL
Column Driver
1366× 768 Pixels
1366×3×768 Cells
Column Driver
X Pulse Generator
Vb
Vcc Vdd Va Vs

Reference

- Vcc : Voltage for Logic Control
- Vdd : Voltage for FET driver
- Va : Voltage for address pulse
- Vsc_l : Voltage sustain low
- Vscan : Voltage for scan high
- Vb : Voltage for X bias
- Vset : Voltage for Y ramp pulse

Figure 6-7 Block diagram (50" HD v3)


Logic Core
Line Difference Detect
Data Control
LVDS
R.G.B
V_sync
H_sync
D_En
DCLK
FIFO
Sync & Data Regenerate
Clock Domain Conversion
R.G.B
SCLK
Image Processing
Dither
Gamma
WB
E/D
R.G.B
Sustain Control
Load Ratio
Driving Signal Control
X Driving Signal
Y Driving Signal
FIFO
Motion Detect
False Contour Reduction
DDR Memory Controller
R.G.B
Subfield conversion
DDR Memory Controller
Rearrange
Address Data
I2C●Logic Interface
u-COM●Logic Interface
Micom
UART
Sync Detect
EXT/INT Detect
Voltage Detect
AC Relay Detect
etc...
DDR Memory (1 Frame storage)
DDR Memory
DDR Memory

F_14991_019.eps
030805

Figure 6-8 Block diagram (50" HD v4)

6.2 PSU Board diagram

6.2.1 PSU 37" SD v4

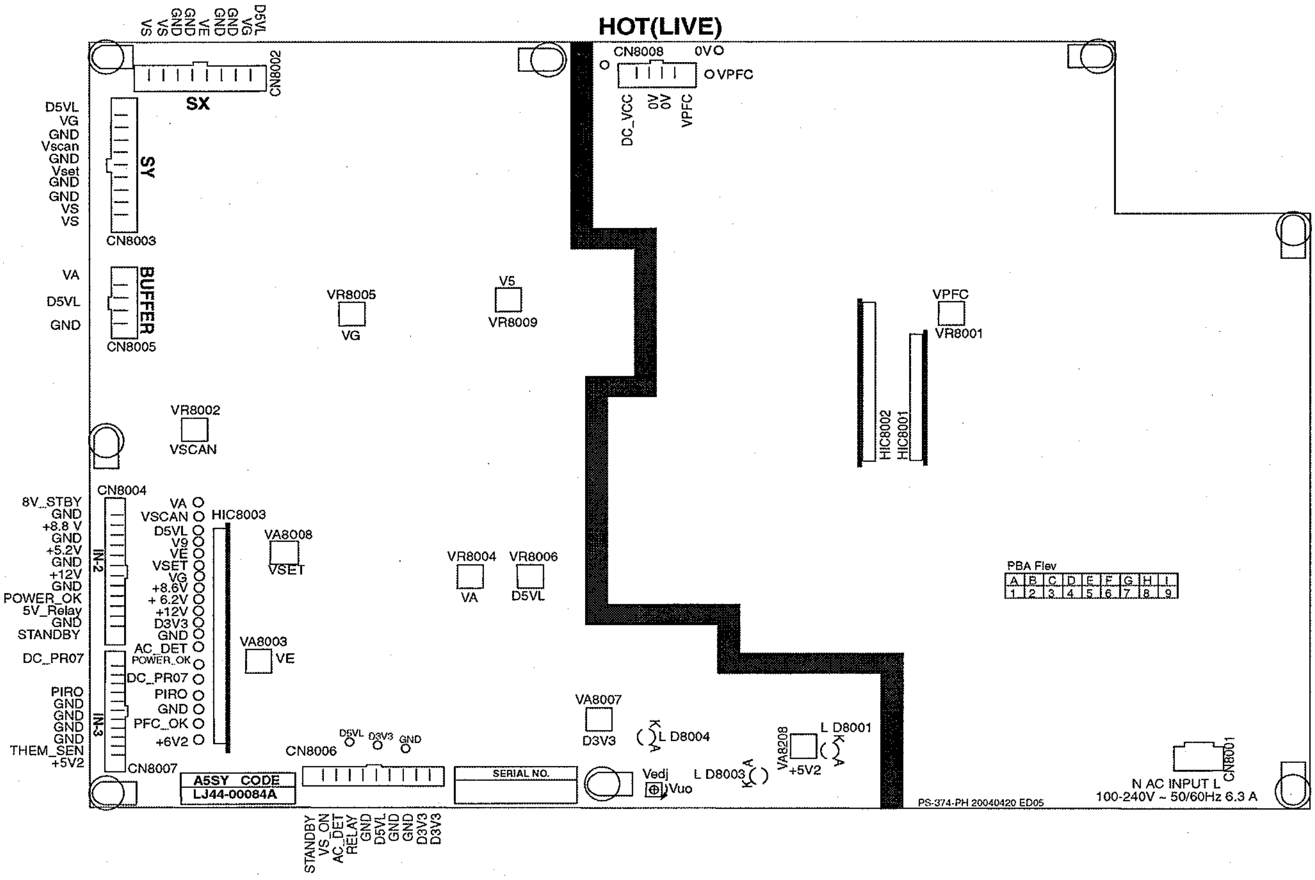

HOT(LIVE)
VS
VS
GND
GND
VE
GND
GND
VG
D5VL
CN8002
SX
D5VL
VG
GND
Vscan
GND
Vset
GND
GND
VS
VS
SY
CN8003
VA
D5VL
GND
BUFFER
CN8005
CN8008
0V
VPFC
DC_VCC
0V
0V
VPFC
VR8005
VG
V5
VR8009
VPFC
VR8001
HIC8002
HIC8001
VR8002
VSCAN
CN8004
8V_STBY
GND
+8.8 V
GND
+5.2V
GND
+12V
GND
POWER_OK
5V_Relay
GND
STANDBY
DC_PR07
PIRO
GND
GND
GND
GND
THEM_SEN
+5V2
IN-2
IN-3
VA
VSCAN
HIC8003
D5VL
V9
VE
VSET
VG
+8.6V
+ 6.2V
+12V
D3V3
GND
AC_DET
POWER_OK
DC_PR07
PIRO
GND
PFC_OK
+6V2
VA8008
VSET
VA8003
VE
VR8004
VA
VR8006
D5VL
PBA Flev
A B C D E F G H I
1 2 3 4 5 6 7 8 9
VA8007
D3V3
K A L D8004
VA8208
L D8001
K A
+5V2
Vedj
Vuo
L D8003
CN8007
A5SY CODE
LJ44-00084A
CN8006
D5VL
D3V3
GND
SERIAL NO.
STANDBY
VS_ON
AC_DET
RELAY
GND
D5VL
GND
GND
D3V3
D3V3
PS-374-PH 20040420 ED05
N AC INPUT L
CN8001
100-240V ~ 50/60Hz 6.3 A

Figure 6-9 PSU layout

Table 6-1 Adjustment voltage level overview

No	Output voltage (V)	Voltage Setting (Nominal Load)	Output Voltage Variable Point
2	VS	170 V	160 V ~ 185 V
3	VA	70V	60 V ~ 80 V
4	VE	180 V	165 V ~ 195 V
5	VSET	173 V	160 V ~ 180 V
6	VSCAN	-160 V	-145 V ~ -175 V
7	D5VL	5.2 V	5.0 V ~ 6.0 V
8	D3V3	3.3 V	2.8 V ~ 3.8 V
9	VCC	15 V	Fixed
10	5V2	5.4 V	4.5 V ~ 5.6 V
11	9V_Standby	8.5 V ~ 9.5 V	Fixed
Check voltage label on the PDP for correct values.			

6.2.2 PSU 42" SD v2

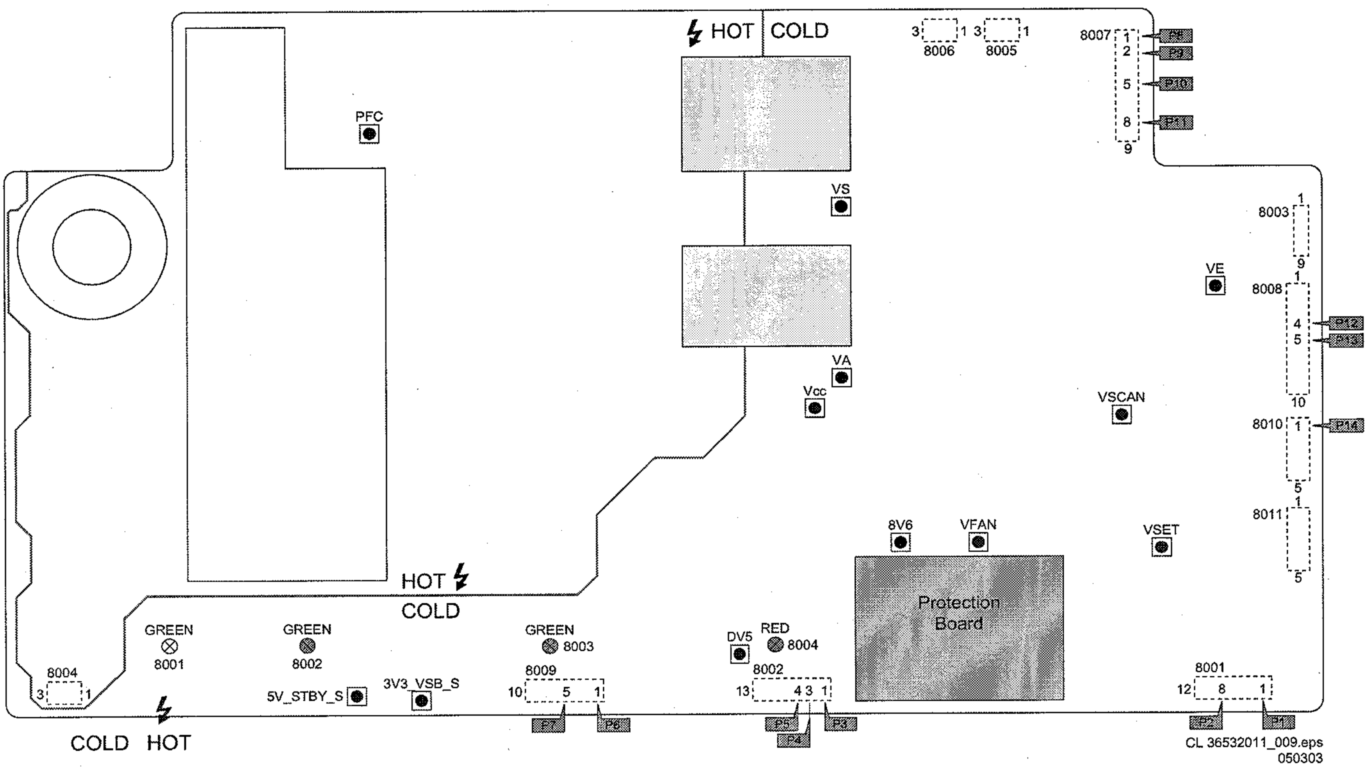

HOT
COLD
3 1 3 1
8006
8005
8007
1
2
5
8
9
P8
P9
P10
P11
PFC
VS
8003
1
9
VE
8008
1
4
5
10
P12
P13
VA
Vcc
VSCAN
8010
1
5
P14
8011
1
5
8V6
VFAN
VSET
Protection Board
HOT
COLD
GREEN
8001
GREEN
8002
GREEN
8003
DV5
RED
8004
8004
3 1
5V_STBY_S
3V3_VSB_S
8009
10 5 1
P7
P6
8002
13 4 3 1
P5
P4
P3
8001
12 8 1
P2
P1
COLD HOT
CL 36532011_009.eps
050303

Figure 6-10 PSU layout

Table 6-2 Adjustment voltage level overview

No	Output voltage (V)	Voltage Setting (Nominal Load)	Output Voltage Variable Point
1	Vs	87V	78V ~ 92V
2	Va	79V	72V ~ 86V
3	Ve	107V	100V ~ 120V
4	Vset	93V	75V ~ 95V
5	Vscan	79V	65V ~ 85V
6	Vg	15V	Fixed
7	D5V	5.2V	5V ~ 5.6V
8	D3V3	3.3V	2.8V ~ 3.7V
Check voltage label on the PDP for correct values.			

6.2.3 PSU 42" SD v3

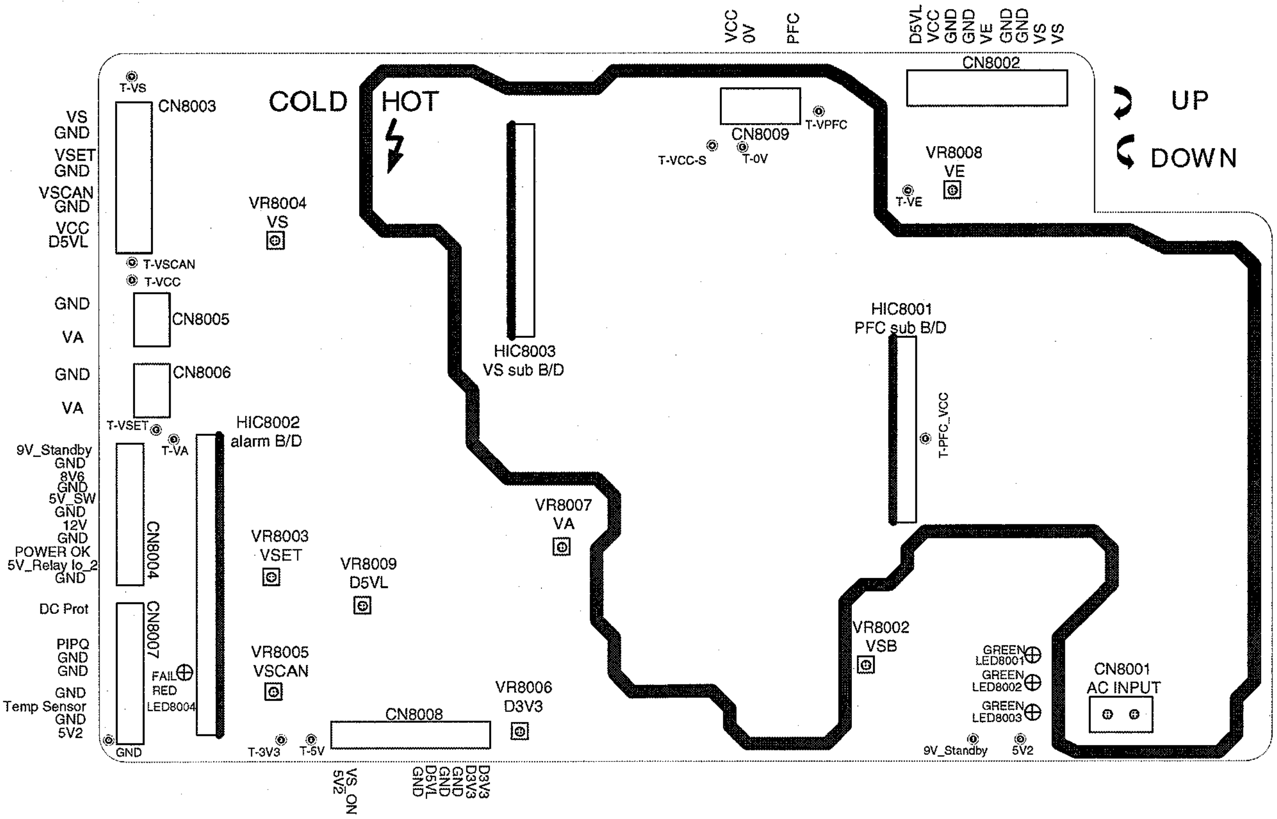
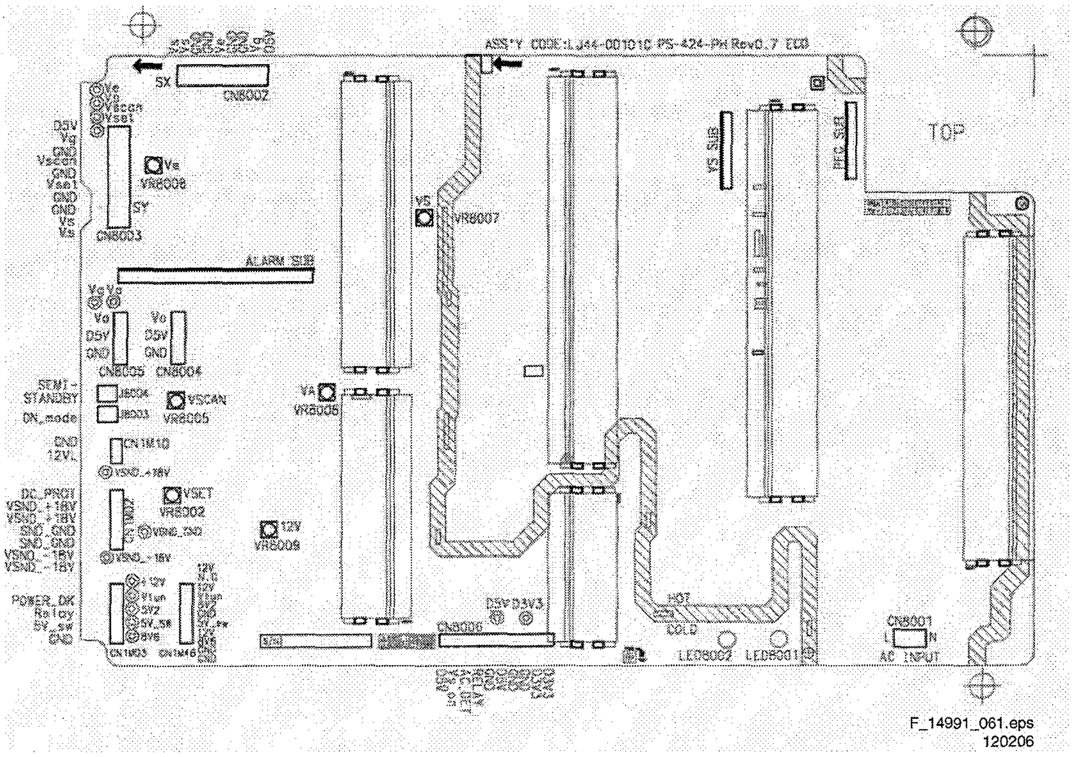

VCC
0V
PFC
D5VL
VCC
GND
GND
VE
GND
GND
VS
VS
CN8002
UP
DOWN
T-VS
CN8003
COLD
HOT
VS
GND
VSET
GND
VSCAN
GND
VCC
D5VL
CN8009
T-VPFC
T-VCC-S
T-0V
VR8008
VE
T-VE
VR8004
VS
T-VSCAN
T-VCC
GND
VA
CN8005
GND
VA
CN8006
HIC8001
PFC sub B/D
HIC8003
VS sub B/D
T-PFC_VCC
T-VSET
T-VA
HIC8002
alarm B/D
9V_Standby
GND
8V6
GND
5V_SW
GND
12V
GND
POWER OK
5V_Relay lo_2
GND
CN8004
VR8007
VA
VR8003
VSET
VR8009
D5VL
DC Prot
CN8007
PIPQ
GND
GND
GND
Temp Sensor
GND
5V2
FAIL
RED
LED8004
VR8005
VSCAN
VR8002
VSB
GREEN
LED8001
GREEN
LED8002
GREEN
LED8003
CN8001
AC INPUT
VR8006
D3V3
CN8008
GND
T-3V3
T-5V
9V_Standby
5V2
VS_ON
5V2
GND
D5VL
GND
GND
D3V3
D3V3

Figure 6-11 PSU layout

Table 6-3 Adjustment voltage level overview

No	Output voltage (V)	Voltage Setting (Nominal Load)	Output Voltage Variable Point
1	Vs	175V	160V ~ 185V
2	Va	70V	65V ~ 80V
3	Ve	160V	150V ~ 170V
4	Vset	173V	160V ~ 18095V
5	Vscan	-60V	-55V ~ -75V
6	D5VL	5.2V	4.0V ~ 6V
7	D3V3	3.3V	5V ~ 5.6V
8	Vcc	15V	Fixed
Check voltage label on the PDP for correct values.			

6.2.4 PSU 42" SD v4


ASS'Y CODE:LJ44-00101C PS-424-PH Rev0.7 ECO
SX
CN8002
Ve
Vs
Vscan
Vset
D5V
Vg
GND
Vscan
GND
Vset
GND
GND
Vs
Vs
Ve
VR8008
SY
CN8003
VS
VR8007
ALARM SUB
Vo
Vo
D5V
GND
Vo
D5V
GND
CN8005
CN8004
SEMI-STANDBY
ON_mode
VSCAN
VR8005
VA
VR8006
GND
12VL
CN1M10
VSND_+18V
DC_PROT
VSND_+18V
VSND_+18V
SND_GND
SND_GND
VSND_-18V
VSND_-18V
VSET
VR8002
VSND_GND
VSND_-18V
12V
VR8009
POWER_OK
Relay
5V_sw
GND
12V
Vtun
5V2
5V_SB
8V6
CN1M03
CN1M46
CN8006
D5V
D3V3
VS SUB
PFC SUB
TOP
HOT
COLD
LED8002
LED8001
CN8001
L
N
AC INPUT

F_14991_061.eps
120206

Figure 6-12 PSU layout

Table 6-4 Adjustment voltage level overview

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Variable Point
1	VS	207V ± 1%	195V ~ 215V
~~2~~	~~VA~~	~~70V ± 1.5%~~	~~50V ~ 70V~~
3	VE	110V ± 1.5%	70V ~ 110V
4	VSET	198V ± 1.5%	180V ~ 210V
5	VSCAN	-185V ± 1.5%	-170V ~ -190V
6	VSB	5V ± 5%	Fixed
7	VG	15V ± 5%	Fixed
8	D5VL	5.2V ± 5%	Fixed
9	D3V3	3.3V ± 5%	Fixed
Check voltage label on the PDP for correct values.			

6.2.5 PSU 42" HD v3

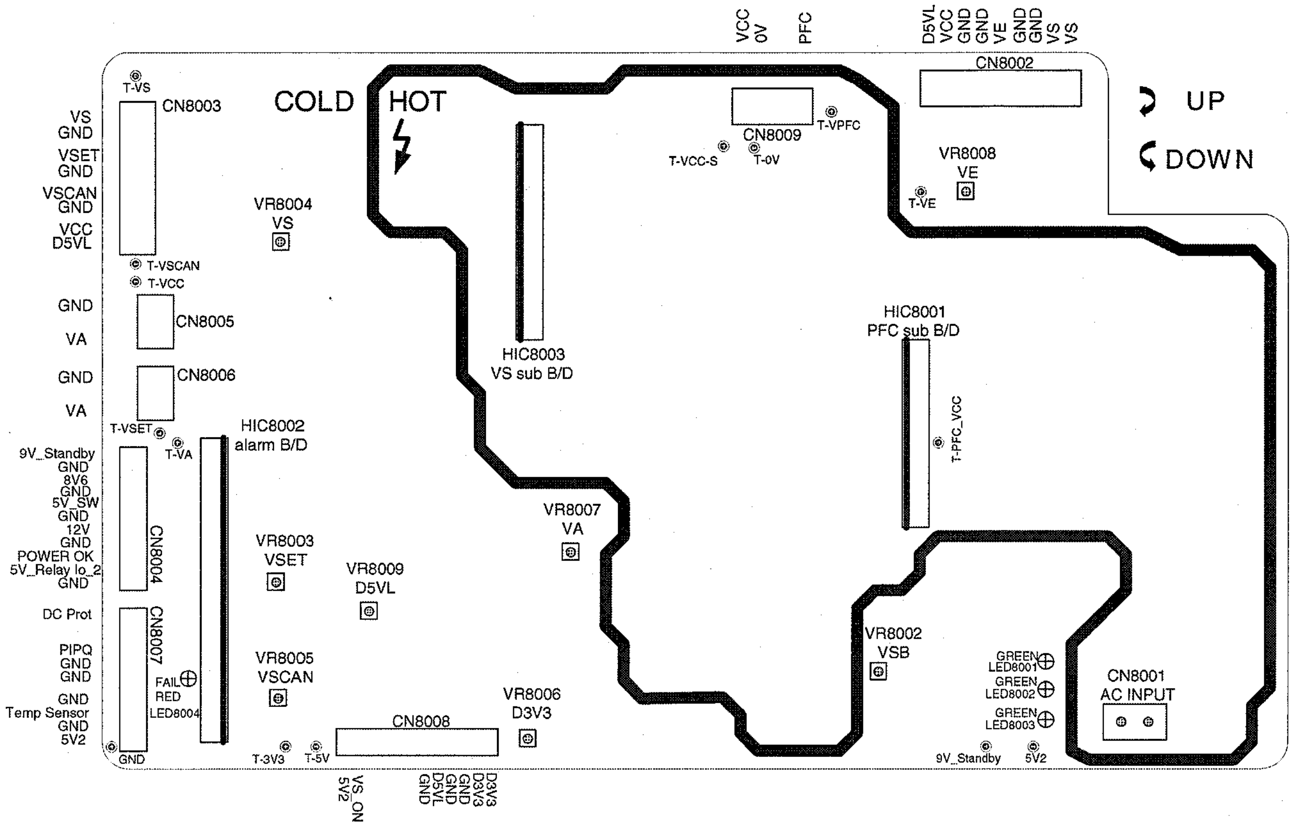
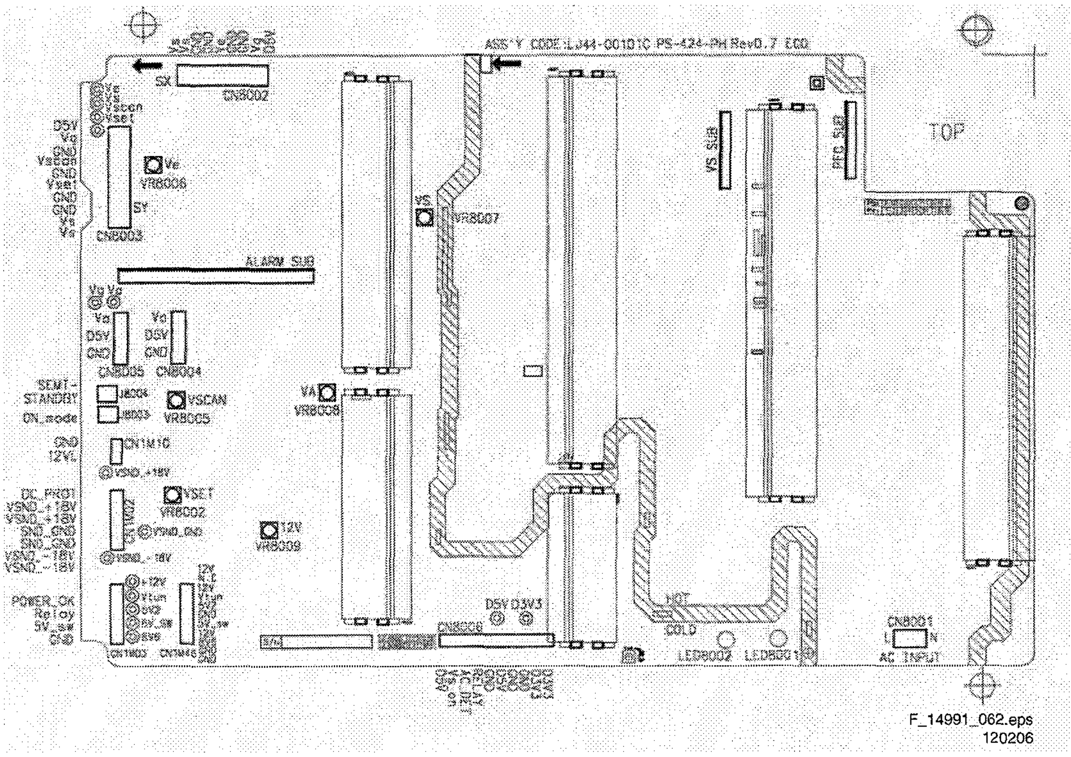

VCC
0V
PFC
D5VL
VCC
GND
GND
VE
GND
GND
VS
VS
CN8002
UP
DOWN
T-VS
CN8003
COLD
HOT
VS
GND
VSET
GND
VSCAN
GND
VCC
D5VL
CN8009
T-VPFC
T-VCC-S
T-0V
VR8008
VE
T-VE
VR8004
VS
T-VSCAN
T-VCC
GND
VA
CN8005
GND
VA
CN8006
HIC8003
VS sub B/D
HIC8001
PFC sub B/D
T-PFC_VCC
T-VSET
T-VA
HIC8002
alarm B/D
9V_Standby
GND
8V6
GND
5V_SW
GND
12V
GND
POWER OK
5V_Relay lo_2
GND
CN8004
VR8007
VA
VR8003
VSET
VR8009
D5VL
DC Prot
CN8007
PIPQ
GND
GND
GND
Temp Sensor
GND
5V2
FAIL
RED
LED8004
VR8005
VSCAN
VR8002
VSB
GREEN
LED8001
GREEN
LED8002
GREEN
LED8003
CN8001
AC INPUT
VR8006
D3V3
CN8008
GND
T-3V3
T-5V
9V_Standby
5V2
VS_ON
5V2
GND
D5VL
GND
GND
D3V3
D3V3

Figure 6-13 PSU layout

Table 6-5 Adjustment voltage level overview

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Variable Point
1	PFC	385V ± 2V	370V ~ 400V
2	VS	175V ± 1%	160V ~ 185V
3	VA	70V ± 1%	65V ~ 80V
4	VE	160V ± 2%	150V ~ 170V
5	VSET	173V ± 2%	160V ~ 180V
6	VSCAN	-60V ± 2%	-55V ~ -75V
7	D5VL	5.2V ± 2%	4.0V ~ 6.0V
8	D3V3	3.3V ± 2%	2.8V ~ 4.0V
9	VCC	15V ± 5%	Fixed
10	5V2	5.4V ± 3%	3.5V ~ 6.0V
11	9V_Standby	8.5V ~ 9.5V	Fixed
Check voltage label on the PDP for correct values.			

6.2.6 PSU 42" HD v4


ASS'Y CODE : LJ44-00101C PS-424-PH Rev0.7 ECO
SX
CN8002
Ve
Vs
Vscan
Vset
D5V
Va
GND
Vscan
GND
Vset
GND
GND
Vs
Vs
Ve
VR8006
SY
CN8003
VS
VR8007
ALARM_SUB
Vg
Va
Va
D5V
GND
CN8005
CN8004
SEMI-STANDBY
ON_mode
J8004
J8003
VSCAN
VR8005
VA
VR8008
GND
12VL
CN1M10
VSND_+18V
DC_PROT
VSND_+18V
VSND_+18V
SND_GND
SND_GND
VSND_-18V
VSND_-18V
VSET
VR8002
VSND_GND
VSND_-18V
12V
VR8009
POWER_OK
Relay
5V_sw
GND
+12V
Vtun
5V2
5V_sw
5V6
CN1M03
CN1M46
D5V D3V3
CN8006
VS_SUB
PFC_SUB
TOP
HOT
COLD
LED8002
LED8001
CN8001
L N
AC INPUT

F_14991_062.eps
120206

Figure 6-14 PSU layout

Table 6-6 Adjustment voltage level overview

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Variable Point
1	Vs	208V	190V ~ 210V
2	Va	70V	50V ~ 70V
3	Ve	90V	80V ~ 105V
4	Vset	195V	180V ~ 205V
5	Vscan	-190V	-170V ~ -205V
6	Vsb	5V	Fixed
7	Vg	15V	Fixed
8	D5VL	5.2V	Fixed
9	D3V3	3.3V	Fixed
Check voltage label on the PDP for correct values.			

6.2.7 PSU 50" HD v3

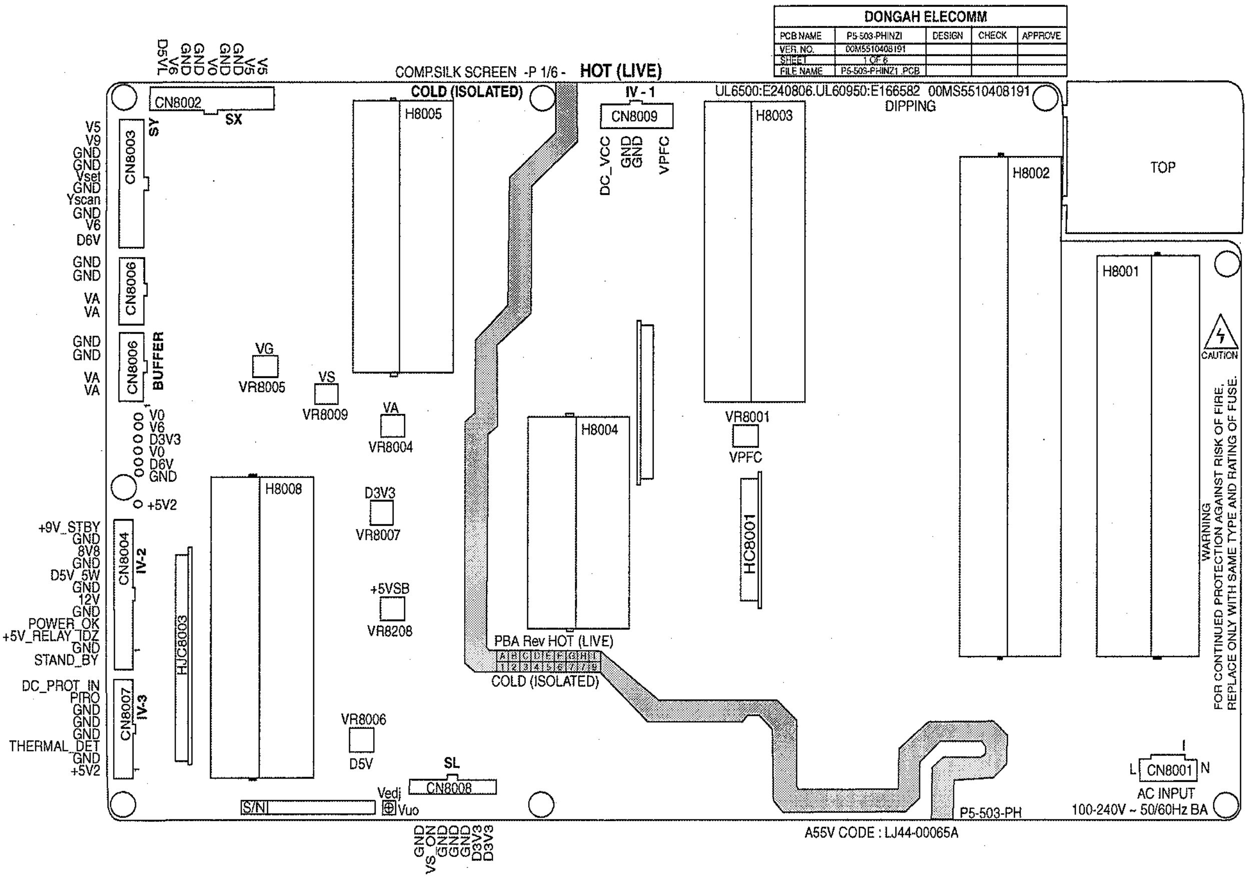
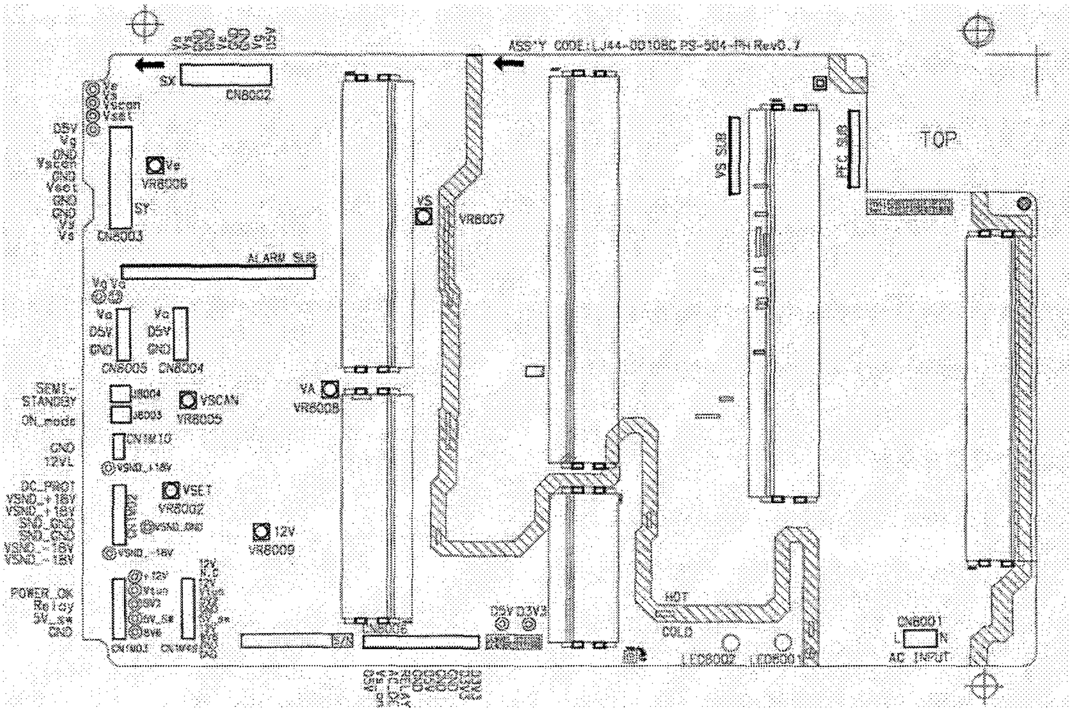

DONGAH ELECOMM
PCB NAME
P5-503-PHINZI
DESIGN
CHECK
APPROVE
VER. NO.
SHEET
FILE NAME
COMP.SILK SCREEN -P 1/6 -
HOT (LIVE)
COLD (ISOLATED)
IV - 1
CN8009
DC_VCC
GND
GND
VPFC
UL6500:E240806.UL60950:E166582 00MS5510408191
DIPPING
TOP
D5VL
V6
GND
GND
VO
GND
GND
V5
CN8002
SX
SY
CN8003
V5
V9
GND
GND
Vset
GND
Yscan
GND
V6
D6V
CN8006
GND
GND
VA
VA
BUFFER
H8005
H8003
H8002
H8001
VG
VR8005
VS
VR8009
VA
VR8004
D3V3
VR8007
+5VSB
VR8208
H8004
H8008
VR8001
VPFC
HC8001
CAUTION
WARNING
FOR CONTINUED PROTECTION AGAINST RISK OF FIRE.
REPLACE ONLY WITH SAME TYPE AND RATING OF FUSE.
V0
V6
D3V3
V0
D6V
GND
+5V2
CN8004
IV-2
+9V_STBY
GND
8V8
GND
D5V_5W
GND
12V
GND
POWER_OK
+5V_RELAY_IDZ
GND
STAND_BY
CN8007
IV-3
DC_PROT_IN
PIRO
GND
GND
GND
THERMAL_DET
GND
+5V2
HJC8003
PBA Rev HOT (LIVE)
A B C D E F G H I
1 2 3 4 5 6 7 8 9
COLD (ISOLATED)
VR8006
D5V
SL
CN8008
Vedj
Vuo
S/N
VS
GND
VO
GND
GND
D3V3
D3V3
P5-503-PH
A55V CODE : LJ44-00065A
CN8001
L
N
AC INPUT
100-240V ~ 50/60Hz BA

Figure 6-15 PSU layout

Table 6-7 Adjustment voltage level overview

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Variable Point
1	PFC	385V ± 2V	370V ~ 400V
2	VS	175V ± 1%	160V ~ 185V
3	VA	70V ± 1%	65V ~ 80V
4	VE	160V ± 2%	150V ~ 170V
5	VSET	173V ± 2%	160V ~ 180V
6	VSCAN	-60V ± 2%	-55V ~ -75V
7	D5VL	5.2V ± 2%	4.0V ~ 6.0V
8	D3V3	3.3V ± 2%	2.8V ~ 4.0V
9	VCC	15V ± 5%	Fixed
10	5V2	5.4V ± 3%	3.5V ~ 6.0V
11	9V_Standby	8.5V ~ 9.5V	Fixed
Check voltage label on the PDP for correct values.			

6.2.8 PSU 50" HD v4


ASS'Y CODE:LJ44-00108C PS-504-PH RevO.7
SX
CN8002
Ve
Vs
Vscan
Vset
D5V
Va
GND
Vscan
GND
Vset
GND
GND
Vs
Vs
Ve
VR8006
SY
CN8003
VS
VR8007
ALARM SUB
Vg Vs
Va
D5V
GND
Va
D5V
GND
CN8005
CN8004
SEMI-STANDBY
ON_mode
J8004
J8003
VSCAN
VR8005
VA
VR8008
GND
12VL
CN1M10
DC_PROT
VSND_+18V
VSND_+18V
SND_GND
SND_GND
VSND_-18V
VSND_-18V
VSET
VR8002
12V
VR8009
POWER_OK
Relay
5V_sw
GND
D5V D3V3
VS SUB
PFC SUB
TOP
HOT
COLD
LED8002
LED8001
CN8001
L
N
AC INPUT

F_14991_063.eps
120206

Figure 6-16 PSU layout

Table 6-8 Adjustment voltage level overview

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Variable Point
1	VS	200V ± 1%	195V ~ 215V
2	VA	70V ± 1.5%	50V ~ 70V
~~3~~	~~VE~~	~~100V ± 1.5%~~	~~70V ~ 110V~~
4	VSET	195V ± 1.5%	180V ~ 210V
5	VSCAN	-175V ± 1.5%	-170V ~ -185V
6	VSB	5V ± 5%	Fixed
7	VG	15V ± 5%	Fixed
8	D5VL	5.2V ± 5%	Fixed
9	D3V3	3.3V ± 5%	Fixed
Check voltage label on the PDP for correct values.			

7. Circuit Diagrams and PWB Layouts

Not applicable.

8. Alignments

Index of this chapter:

8.1 Alignments 37” SD v4
8.2 Alignments 42” SD v2
8.3 Alignments 42” SD v3
8.4 Alignments 42” HD v3
8.6 Alignments 42” HD v4
8.7 Alignments 50” HD v3
8.8 Alignments 50” HD v4
8.9 Alignment value overview (all screens)

Note:

- Figures can deviate due to the different model executions.

Important: Remove all non-default jumpers and reset all DIP switches, after the repair!

8.1 Alignments 37” SD v4

1. Set the pattern to Full White (place jumper CN2008 on the Logic Board).
2. Set Vsch (see Figure “Test point location LJ92-0102A”) to -38V (see Figure “Waveform adjustment (Y-Board)”). Check with a digital multimeter, connected between the Y-scan test point and ground. Adjust the voltage with VR5000.
3. Check the waveform using an Oscilloscope.
    - Triggering through V_TOGG of the LOGIC Board (see Figure “Logic PWB”).
    - Connect the “ODD” test point, located at the centre of Y_buffer (see Figure “Potentiometer locations LJ92-01149A”), to the other channel, and then check the first Subfield waveform of one TV-Field.
    - Check the waveform by adjusting Horizontal Division of the oscilloscope.
4. Adjust the flat time of the rising ramp of the 1st subframe to 40 µS with VR5001 (see Figure “Rising ramp flat time adjustment”).
5. Adjust the flat time of the falling ramp of the 1st subframe to 16 µs with VR5002 (see Figure “Falling ramp flat time adjustment”).
    - This is a difficult adjustment.
    - It is easier and more accurate to do the following:
        - Count 3 pulses between A and B;
        - Set the difference between A and B to 40 V; the time between C and D will then automatically be set to approximately 16 µS
        - Settings of the oscilloscope: vertically 20VDC/div, horizontally 10 µS/div.
6. Check with the oscilloscope if the voltage of Vsch is -38 V (see Figure “Y-scan H waveform”).

Special notice: It is very important, that you execute this adjustment on the 1st Sub-Field (SF) of the 1st Frame of the Reset waveform and then move to the 3rd Sub-field for adjusting.

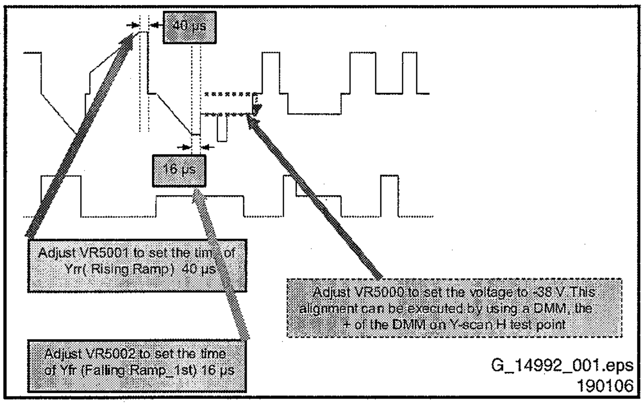

40 µs
16 µs
Adjust VR5001 to set the time of Yrr(Rising Ramp) 40 µs
Adjust VR5000 to set the voltage to -38 V. This alignment can be executed by using a DMM, the + of the DMM on Y-scan H test point
Adjust VR5002 to set the time of Yfr (Falling Ramp_1st) 16 µs
G_14992_001.eps
190106

Figure 8-1 Waveform adjustment (Y-Board)

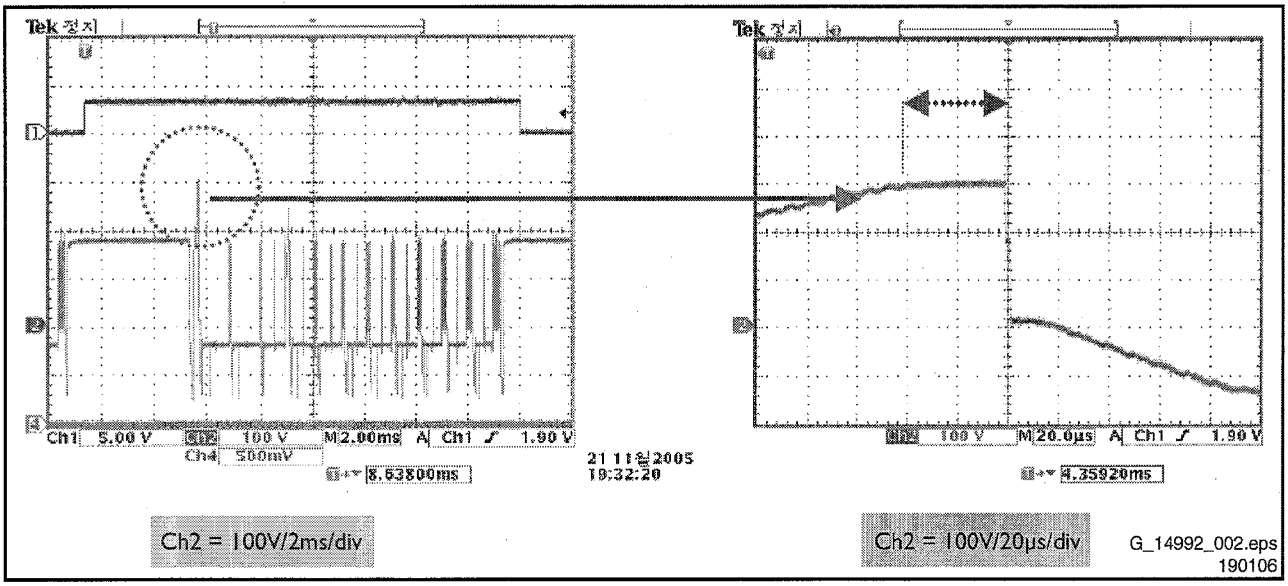
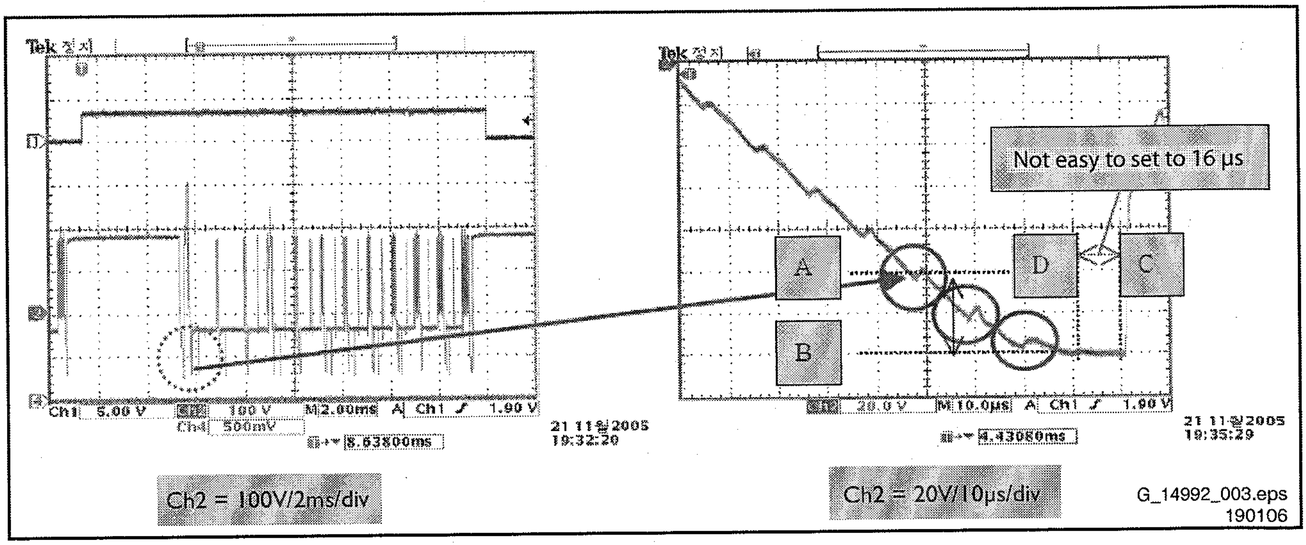

Tek 정지
Ch1 5.00 V
100 V
M 2.00ms
A Ch1 ∫ 1.90 V
Ch4 500mV
8.63800ms
21 11월2005
19:32:20
Tek 정지
100 V
M 20.0µs
A Ch1 ∫ 1.90 V
4.35920ms
Ch2 = 100V/2ms/div
Ch2 = 100V/20µs/div
G_14992_002.eps
190106

Figure 8-2 Rising ramp flat time adjustment (Y-Board)

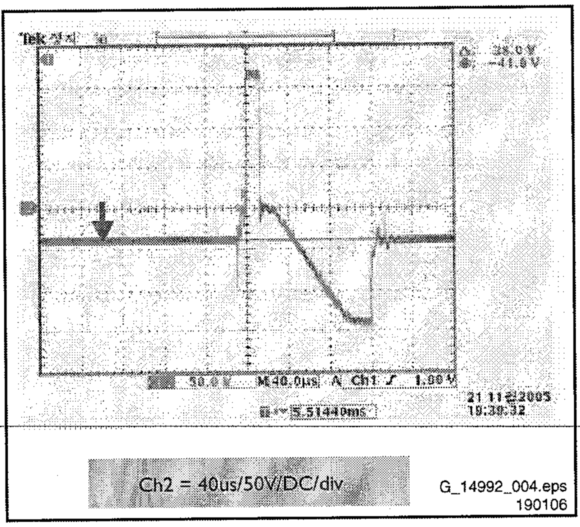


Ch2 = 100V/2ms/div

Ch2 = 20V/10µs/div

G_14992_003.eps
190106

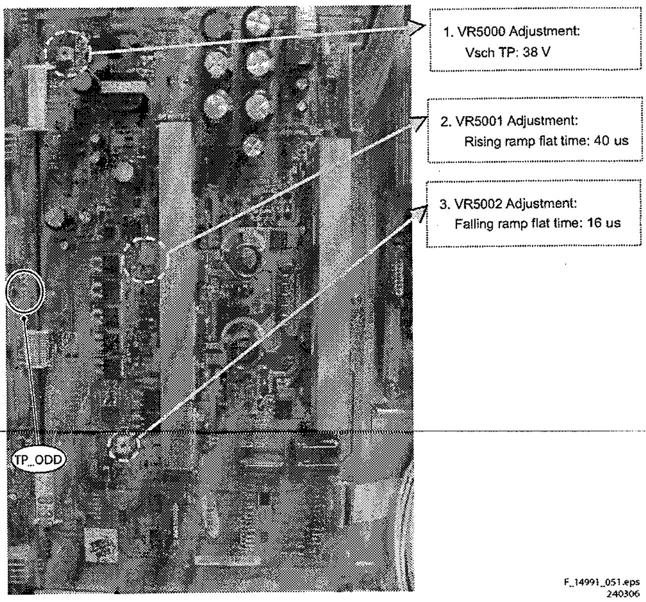
Figure 8-3 Falling ramp flat time adjustment (Y-Board)



Ch2 = 40us/50V/DC/div

G_14992_004.eps
190106

Figure 8-4 Y-scan H waveform (Y-Board)



1. VR5000 Adjustment:
Vsch TP: 38 V

2. VR5001 Adjustment:
Rising ramp flat time: 40 us

3. VR5002 Adjustment:
Falling ramp flat time: 16 us

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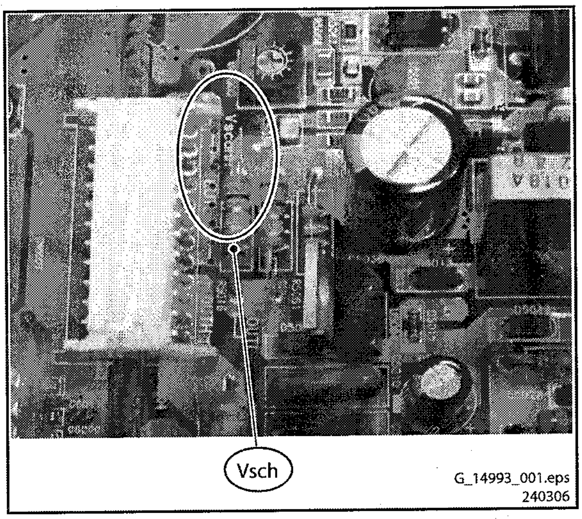
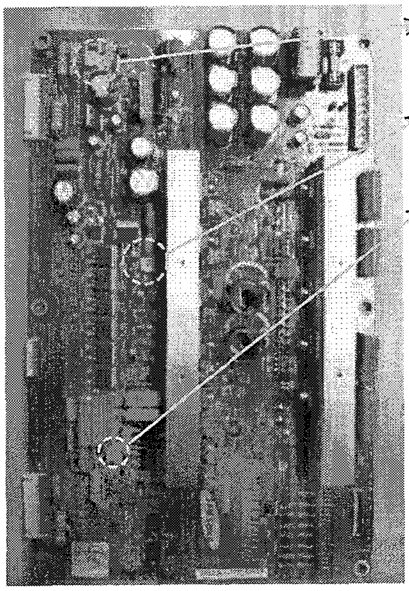
240306

Figure 8-6 Potentiometer locations LJ92-01149A



G_14993_001.eps
240306

Figure 8-5 Test point location LJ92-01021A



1. VR5000 Adjustment:
Vsch TP: 38 V

2. VR5001 Adjustment:
Rising ramp flat time: 40 us

3. VR5002 Adjustment:
Falling ramp flat time: 16 us

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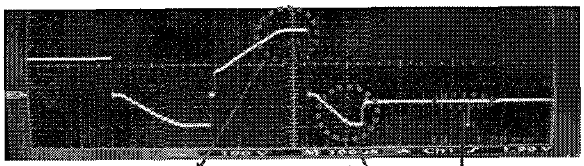
140206

Figure 8-7 Potentiometer locations LJ92-01149B



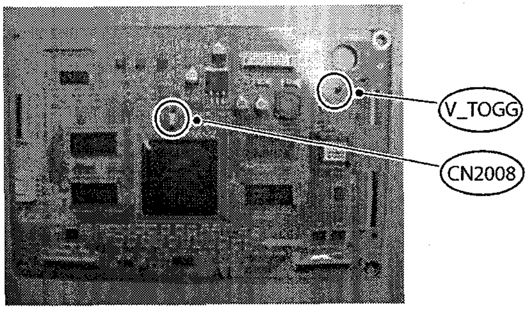
Adjust VR5001 to set the time of Yrr(Rising Ramp) 30㎲

Adjust VR5002 to set the time of Yfr(Falling Ramp) 16㎲

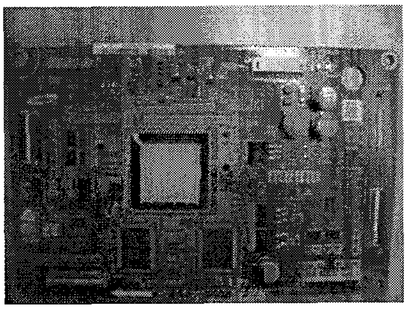
Adjust VR5000 to set the Voltage of Vsch -38V

G_14991_066.eps
140206

Figure 8-8 Wave form adjustment (Y-Main board)



LJ92-01056A / LJ92-01145A

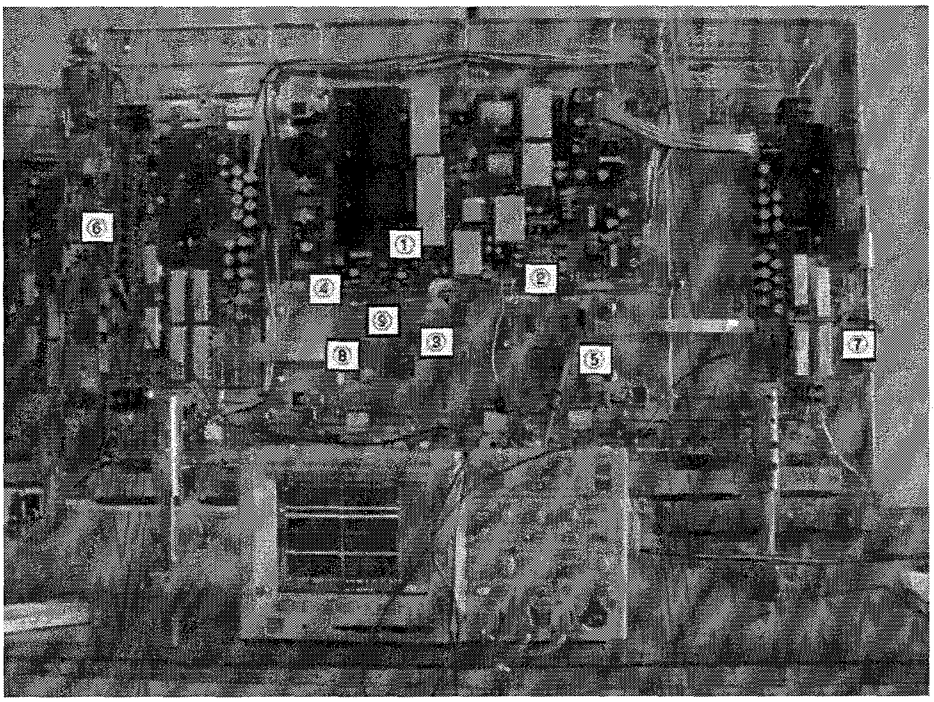


LJ92-01057A

F_14991_068.eps
230306

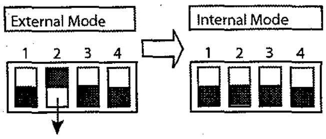
Figure 8-9 Logic PWB

8.2 Alignments 42" SD v2



1) *Preparation*

1 Insert jumper J8002 on PSU board
2 Connect the Jig connector switch
3 Put the Logic board dipswitches into internal mode, to generate a Full White screen



4 Connect the AC power jig

Connect the Oscilloscope:

5 CH1: V-SYNC (CN201)
6 CH2: Y-output (OUT4)
7 CH3: X-output (TP OUT)
8 Connect the Key-scan Board

2) Turn-On.

- *Turn on the Power switch*
- Check the LED on the Logic Board
- Check waveform of X- and Y-board (Refer to Picture below)

Figure 8-10 Adjusting procedure (42" SD v2)

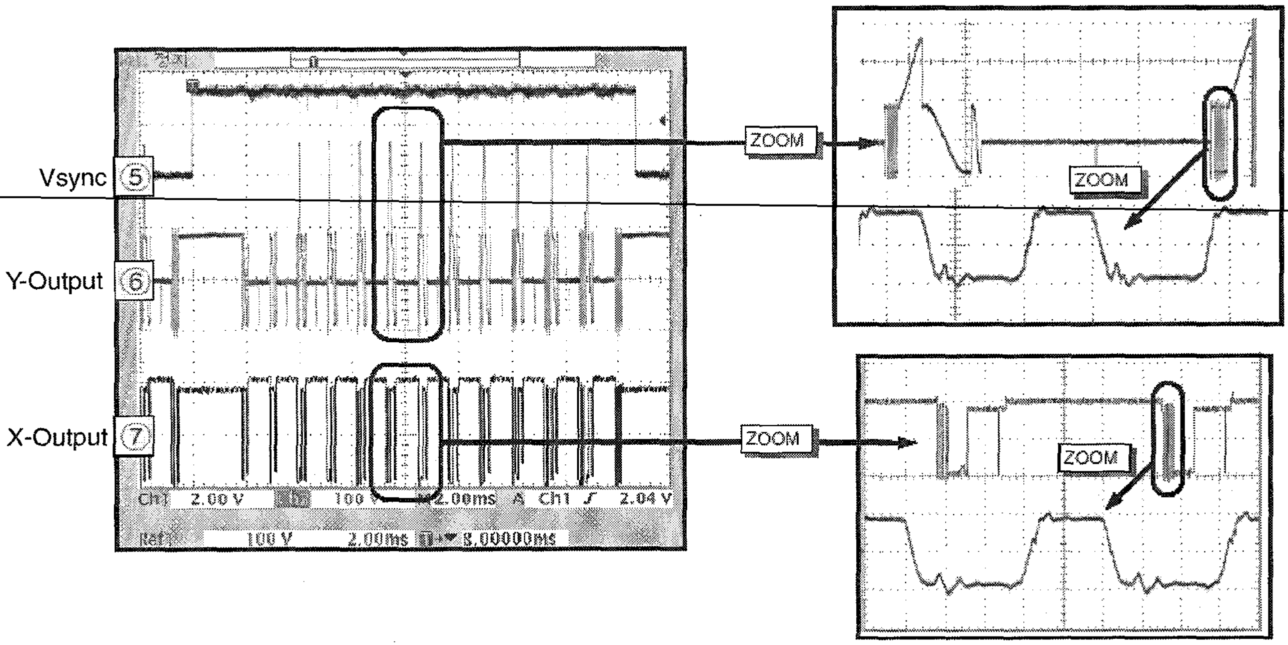
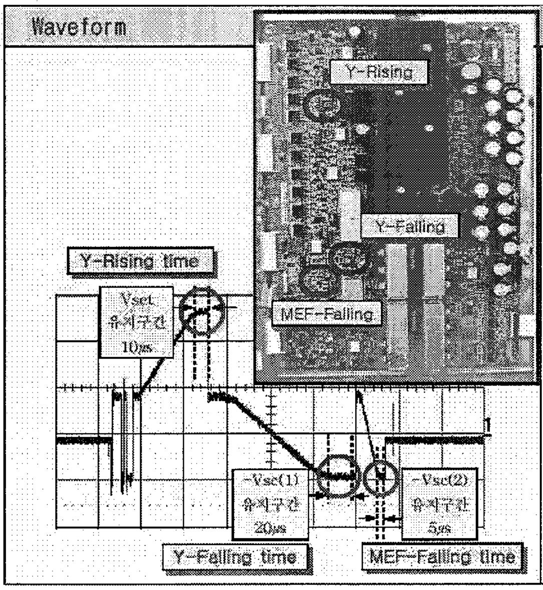


Figure 8-11 Waveform of X- and Y-board (42" SD v2)


Waveform
Y-Rising
Y-Falling
MEF-Falling
Y-Rising time
Vset 유지구간 10μs
1
-Vsc(1) 유지구간 20μs
-Vsc(2) 유지구간 5μs
Y-Falling time
MEF-Falling time

Procedure

1) Make Full White on Screen.

2) Observe waveform using Oscilloscope.

a Check OUT4 TP in Y-buffer(upper).
Observe the waveform of the third waveform of 1TV-Field.
b Adjust the division of oscilloscope like the left picture
c Adjust the period of Vset as 10μS, that of -Vsc(1) as 20μs, that of -Vsc(2) as 5μs, turning VR (Variable Resistor) (only,when you adjust each period of -Vsc(1) & -Vsc(2) adjust Vertical Division of oscilloscope as '2V or 5V')
d VR for Vset : VR5003 (Y_main)
VR for -Vsc(1) : VR5001 (Y_main)
VR for -Vsc(2) : VR5002 (Y_main)

Figure 8-12 How to adjust the waveform (42" SD v2)

8.3 Alignments 42" SD v3

1. Put the dipswitches on the Logic Board in the internal position to get a Full White Pattern.
2. You can find the location of the test point and potentiometers in Figure "Potentiometer locations".
3. Adjust Vsch to 40 V with VR5004.
4. Check the waveform with an Oscilloscope.
   - Take the trigger signal from the testpoint marked "V-sync" on the Logic Board.
   - Connect the testpoint marked "OUT 4", located in the centre of Y_buffer Board to the other channel, and then check the first Subfield operating waveform of one TV-Field.
   - Check the waveform again after adjusting Horizontal Division. Check the Reset waveform when the V_TOGG Level is changed.
   - Set the Vset to 10µs by adjusting VR5002.
   - Set the Falling maintenance time to 30 µs by adjusting VR5003.
   - Change the waveform position of Oscilloscope to the 3rd Subfield and then set the Falling maintenance time to 30µsby adjusting the VR5001. GND maintenance section should be checked after the Vertical Division is readjusted to '2 V or 5 V'.

Special notice: It is very important, that you execute this adjustment on the 1st Sub-Field (SF) of the 1st Frame of the Reset waveform and then move to the 3rd Sub-field for adjusting.

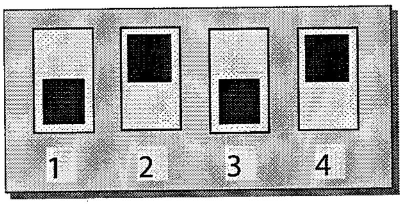


Figure 8-13 DIP switch mode: External

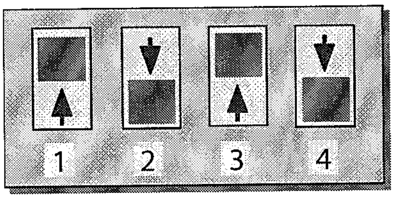


Figure 8-14 DIP switch mode: Internal

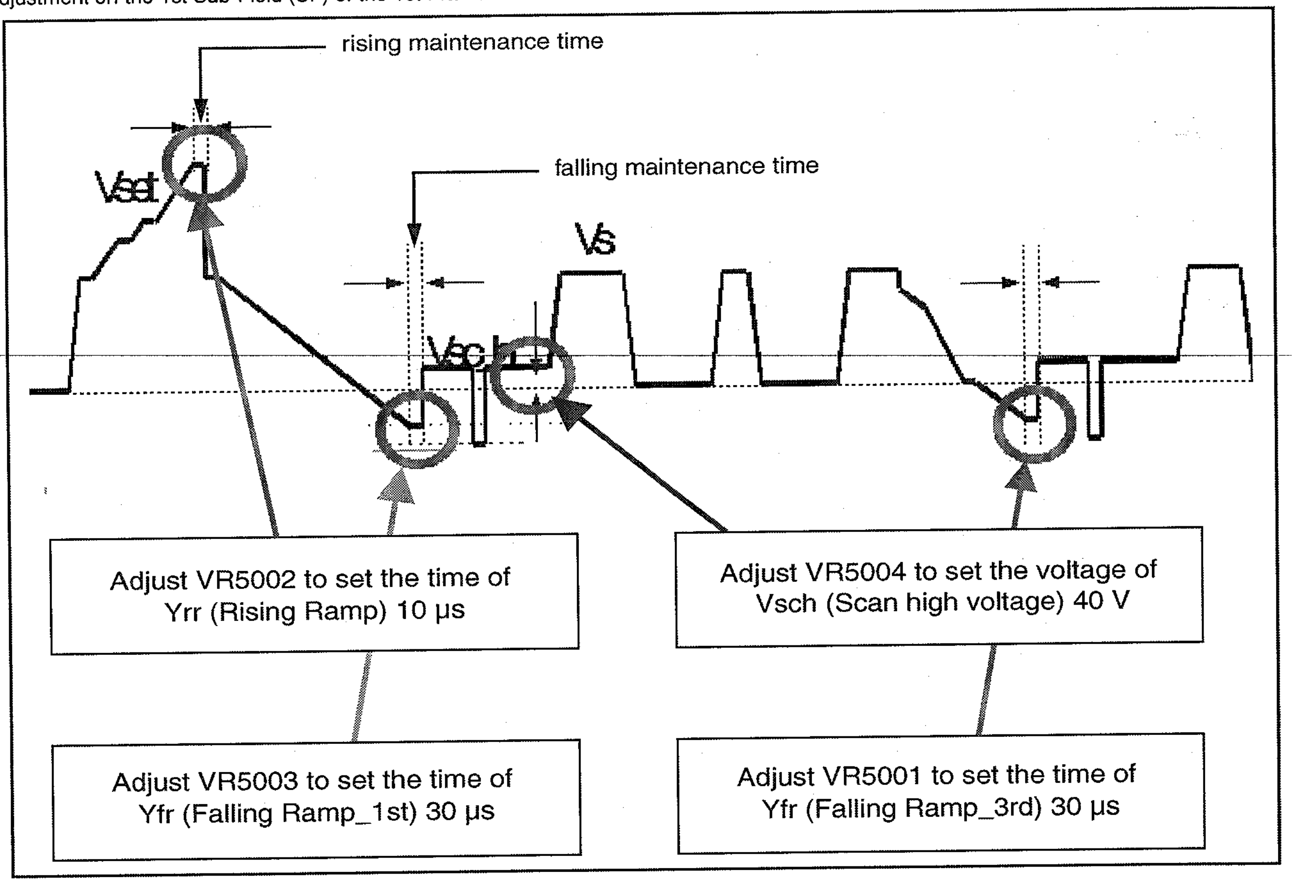

rising maintenance time
falling maintenance time
Vset
Vs
Vsch
Adjust VR5002 to set the time of Yrr (Rising Ramp) 10 µs
Adjust VR5004 to set the voltage of Vsch (Scan high voltage) 40 V
Adjust VR5003 to set the time of Yfr (Falling Ramp_1st) 30 µs
Adjust VR5001 to set the time of Yfr (Falling Ramp_3rd) 30 µs

Figure 8-15 TCP ramp waveform inclination adjustment (Y-Board)

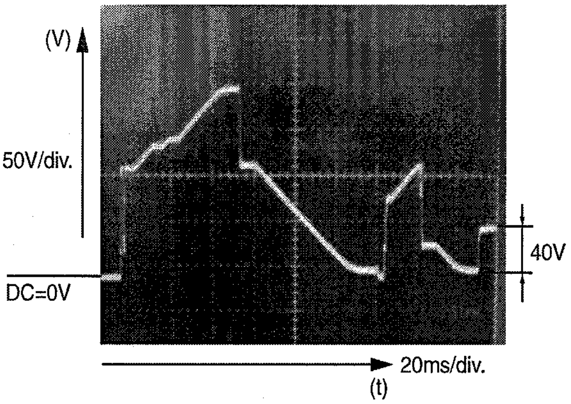


Figure 8-16 Rising ramp

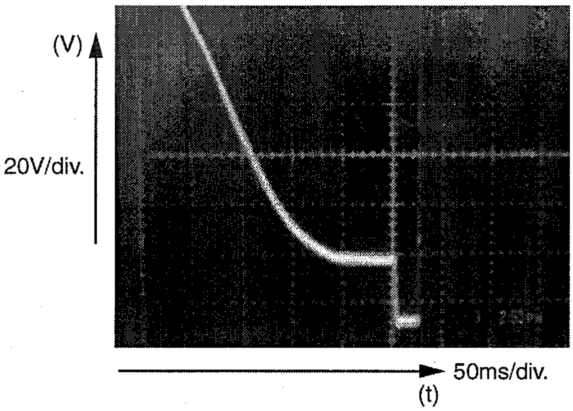
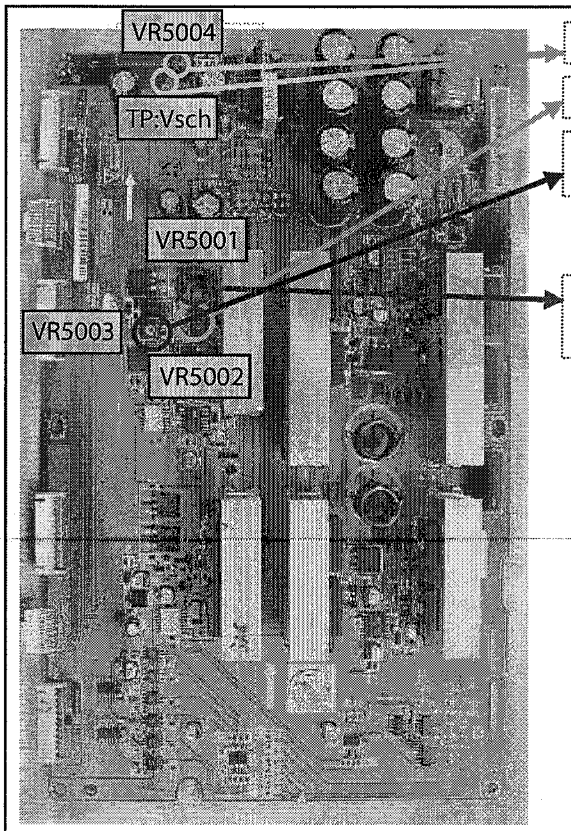


Figure 8-17 Falling ramp



1. VR5004 Adjustment: Vsch TP => 40 volt

2. VR5002 Adjustment: Rising Ramp flat time: Typ. 10 μsec

3. VR5003 Adjustment: Falling Ramp flat time => Typ. 30 μsec

4. VR5001 Adjustment: 3rd SF Falling Ramp flat time => Typ. 30 μsec

* Pay close attention to above adjustment

Figure 8-18 Potentiometer locations

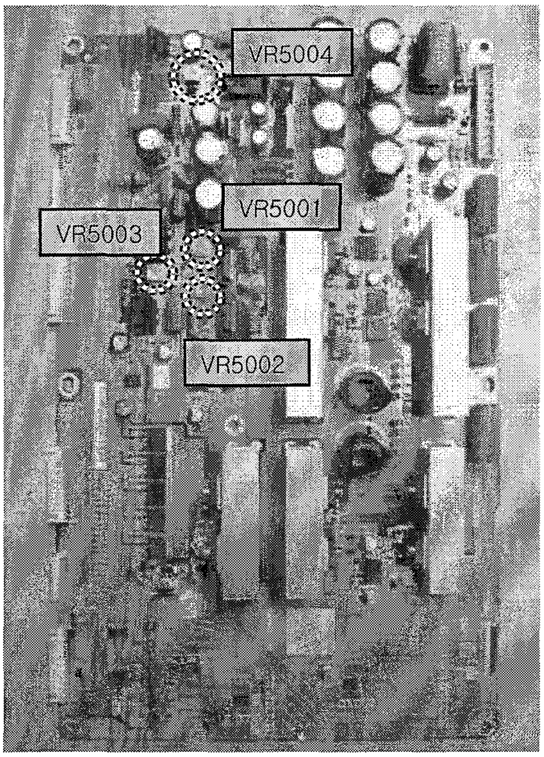

VR5004
VR5001
VR5003
VR5002
LJ92-01284A
F_14991_070.eps
140206

Figure 8-19 Potentiometer locations LJ92-01284A

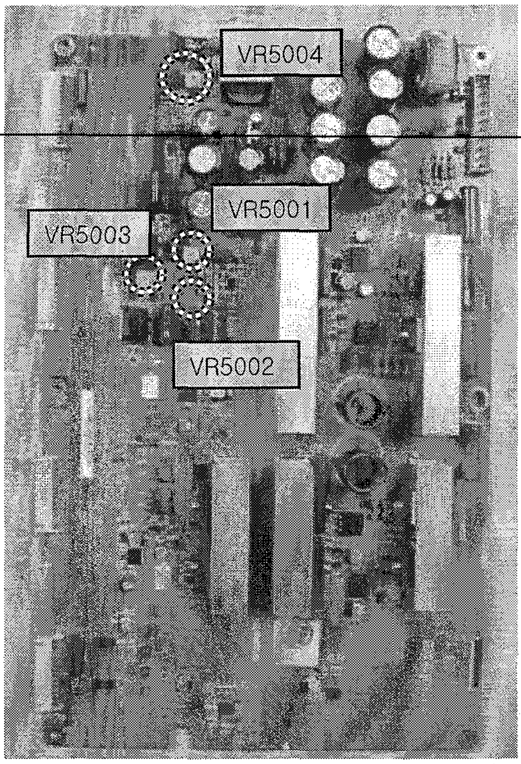

VR5004
VR5001
VR5003
VR5002
LJ92-00944B
F_14991_069.eps
140206

Figure 8-20 Potentiometer locations LJ92-00944B

8.4 Alignments 42" HD v3

1. Put the dipswitches on the Logic Board in the internal position to get a Full White Pattern.
2. Adjust Vsch to Clock-wise max by using VR5004 (Vsch should be connected to "+" unit of DMM).
3. Check the waveform using Oscilloscope.
   - Triggering through V_TOGG of LOGIC Board.
   - Connect the OUT 4 Test Point at the centre of Y_buffer to other channel, and then check the first Subfield operating waveform of one TV-Field.
   - Check the waveform again after adjusting Horizontal Division. Check the Reset waveform when the V_TOGG Level is changed.
   - Set the Vset to 20 µs by adjusting VR5002. GND maintenance section should be checked after the Vertical Division is readjusted to '2 V or 5 V'.
   - Set the Falling maintenance time to 20 µs by adjusting VR5006.
   - Change the waveform position of Oscilloscope to the 3rd Subfield and then set the Falling maintenance time to 10µs by adjusting the VR5003. GND maintenance section should be checked after the Vertical Division is readjusted to '2 V or 5 V'.

Special notice: It is very important, that you execute this adjustment on the 1st Sub-Field (SF) of the 1st Frame of the Reset waveform and then move to the 3rd Sub-field for adjusting.

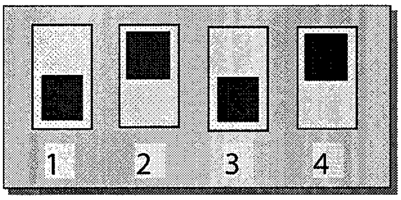


Figure 8-21 DIP switch mode: External

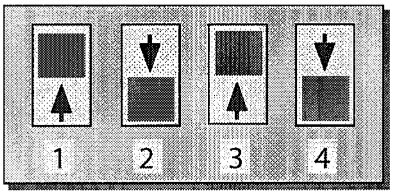


Figure 8-22 DIP switch mode: Internal

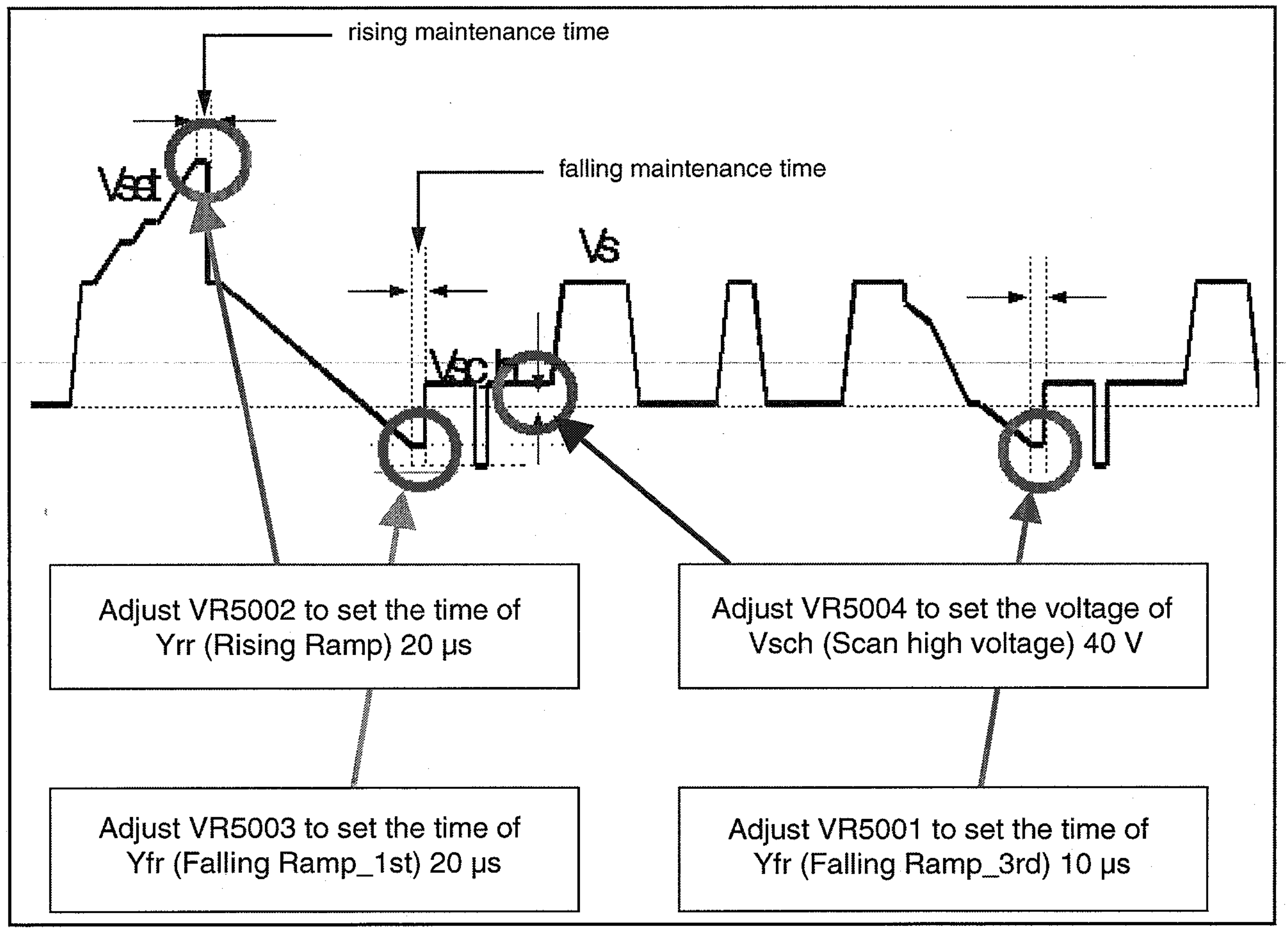

rising maintenance time
Vset
falling maintenance time
Vs
Vsch
Adjust VR5002 to set the time of Yrr (Rising Ramp) 20 µs
Adjust VR5004 to set the voltage of Vsch (Scan high voltage) 40 V
Adjust VR5003 to set the time of Yfr (Falling Ramp_1st) 20 µs
Adjust VR5001 to set the time of Yfr (Falling Ramp_3rd) 10 µs

Figure 8-23 TCP ramp waveform inclination adjustment (Y-Board)

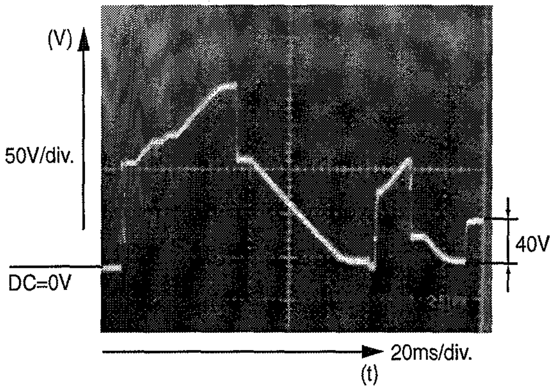


Figure 8-24 Rising ramp

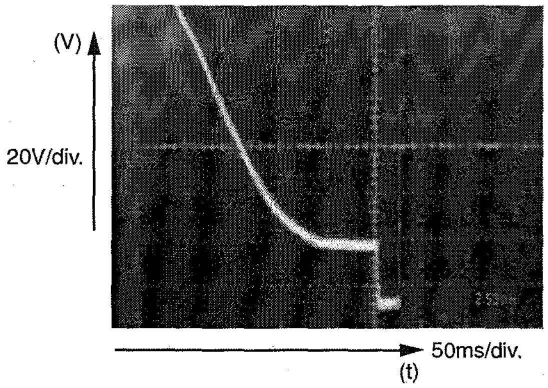
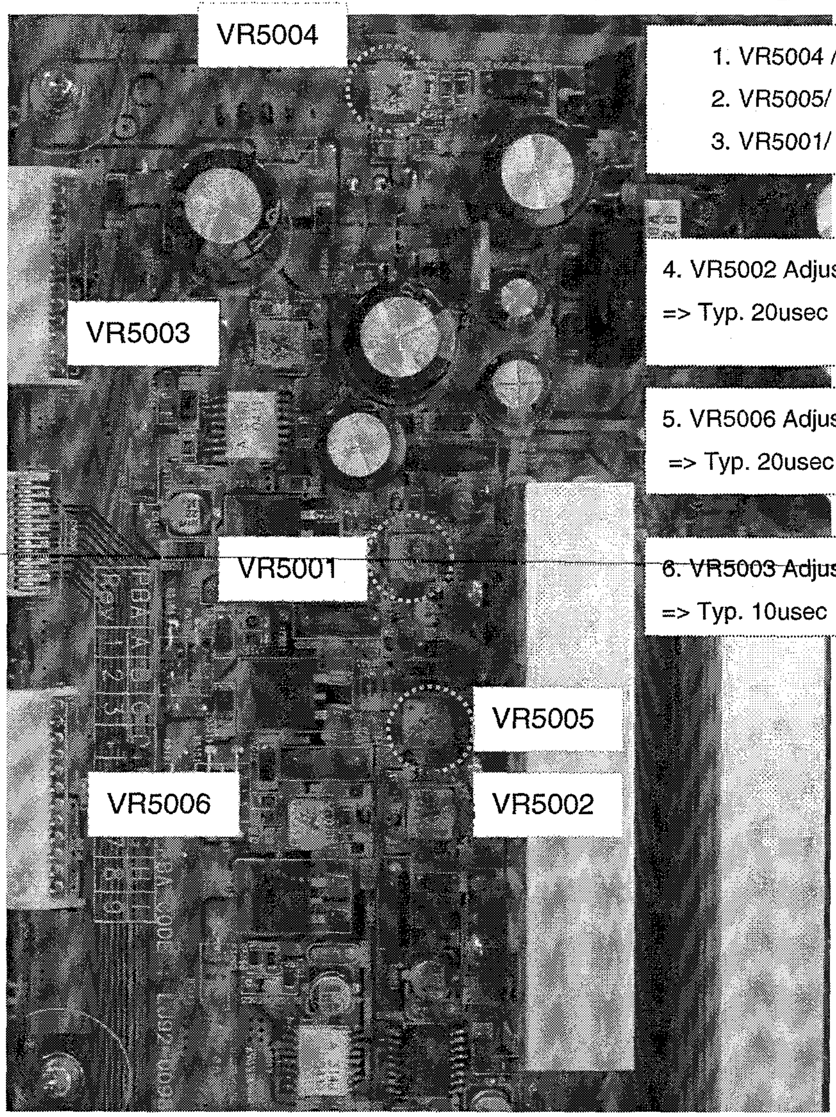


Figure 8-25 Falling ramp



1. VR5004 / Adjustment; Clock-wise to max
2. VR5005/ Adjustment; Clock-wise to max
3. VR5001/ Adjustment; Clock-wise to 4 th division

4. VR5002 Adjustment: Rising Ramp flat time:
=> Typ. 20usec

5. VR5006 Adjustment: Falling Ramp flat time
=> Typ. 20usec

6. VR5003 Adjustment: 3th SF Falling Ramp flat time
=> Typ. 10usec

* Pay close attention to above adjustment

Figure 8-26 Potentiometer locations

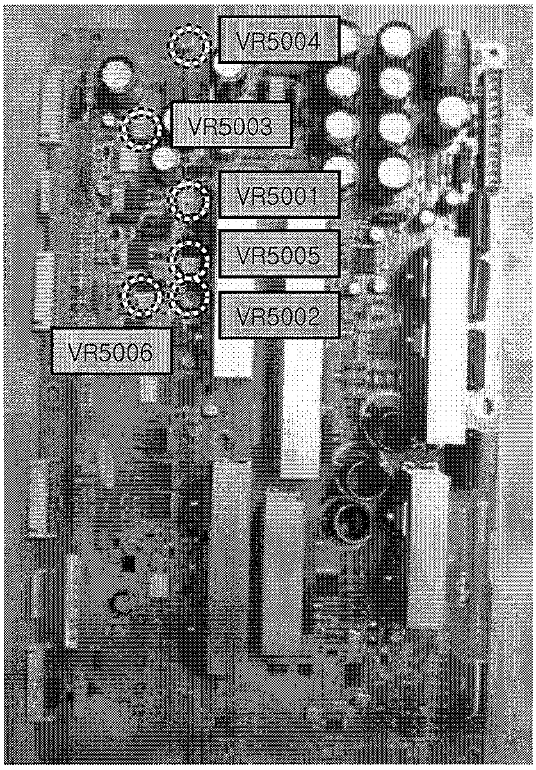

VR5004
VR5003
VR5001
VR5005
VR5002
VR5006
LJ92-00981A
F_14991_071.eps
140206

Figure 8-27 Potentiometer locations LJ92-00981A

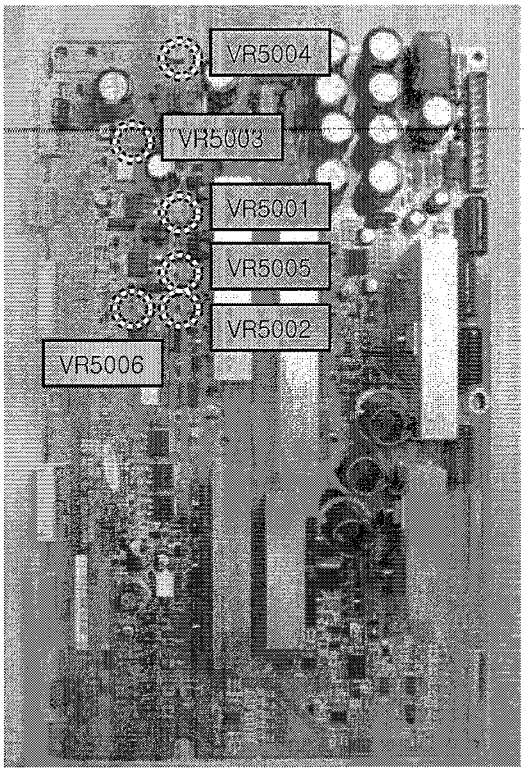
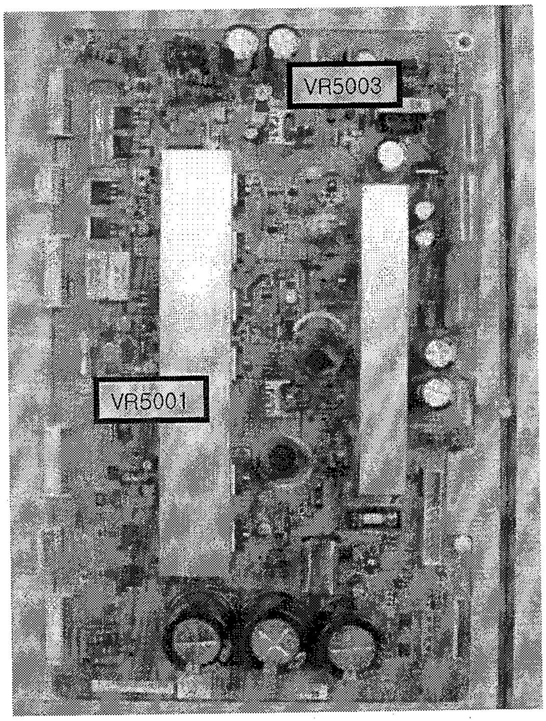

VR5004
VR5003
VR5001
VR5005
VR5002
VR5006
LJ92-00981B
F_14991_072.eps
140206

Figure 8-28 Potentiometer locations LJ92-00981B

8.5 Alignments 42" SD v4

1. Get Pattern to be Full White (place jumper CN2034 on Logic Board).
2. Check the waveform using an Oscilloscope.
    - Triggering through V_TOGG of LOGIC Board.
    - Connect the OUT 240 Test Point at the centre of Y_buffer to other channel, and then check the first aid-reset waveform from the last sustain of 1TV-Field.
    - Check the waveform again after adjusting Horizontal Division.
      Check the Reset waveform when the V_TOGG Level is changed.
    - Adjust the flat time of the rising ramp to 60µs with VR5001.
    - Adjust the flat time of the falling ramp to 80µs with VR5003.



LJ92-01337A

1.VR5001 Adjustment : Rising Ramp flat time : → 60 µs

2.VR5003 Adjustment : Falling Ramp flat time : → 80 µs

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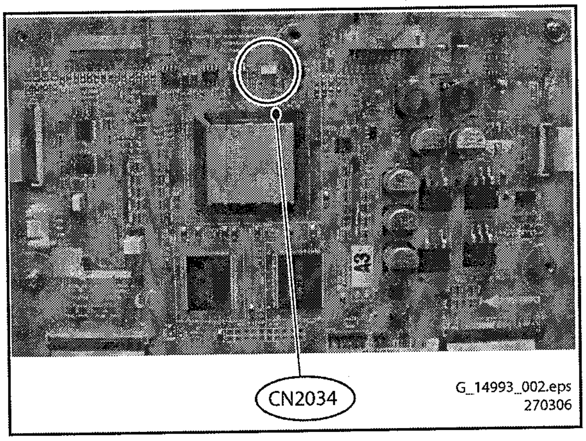
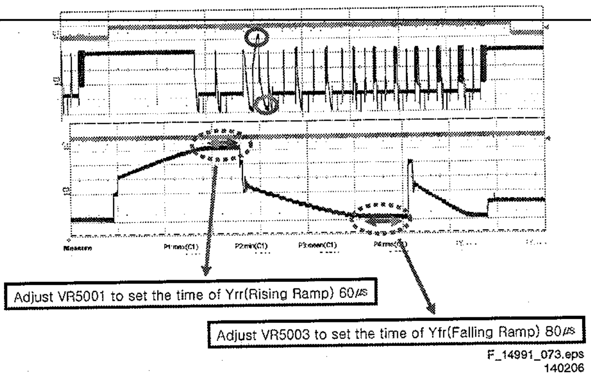
140206

Figure 8-29 Potentiometer locations



G_14993_002.eps
270306

Figure 8-30 Jumper location (Logic board)



Adjust VR5001 to set the time of Yrr(Rising Ramp) 60µs

Adjust VR5003 to set the time of Yfr(Falling Ramp) 80µs

F_14991_073.eps
140206

Figure 8-31 Wave form adjustment (Y-Main board)

8.6 Alignments 42” HD v4

1. Get Pattern to be Full White (place jumper CN2072 on Logic Board).
2. Check the waveform using an Oscilloscope.
    - Triggering through V_TOGG of LOGIC Board.
    - Connect the OUT 240 Test Point at the centre of Y_buffer to other channel, and then check the first aid-reset waveform from the last sustain of one TV-Field.
    - Check the waveform again after adjusting Horizontal Division.
      Check the Reset waveform when the V_TOGG Level is changed.
    - Set the 15V by adjusting VR5002.
    - Set the 100V and 50us by adjusting VR5001

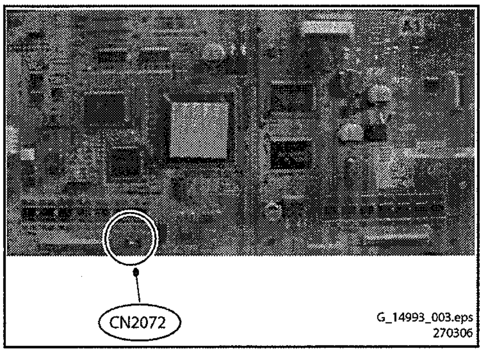
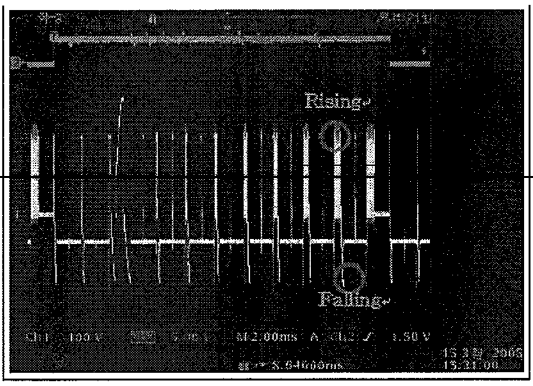
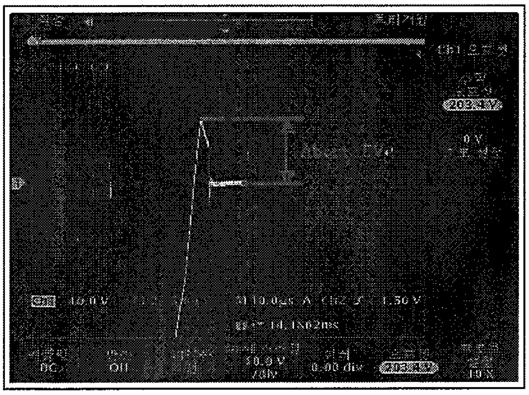

CN2072
G_14993_003.eps
270306

Figure 8-32 Jumper location (Logic board)


Rising
Falling

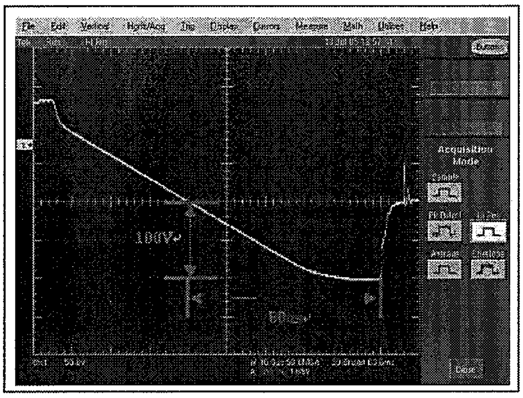
F_14991_023.eps
030805

Figure 8-33 1st subfield from the last sustain within 1 frame



F_14991_024.eps
030805

Figure 8-34 Rising ramp of aid-reset



F_14991_025.eps
030805

Figure 8-35 Falling ramp of aid-reset

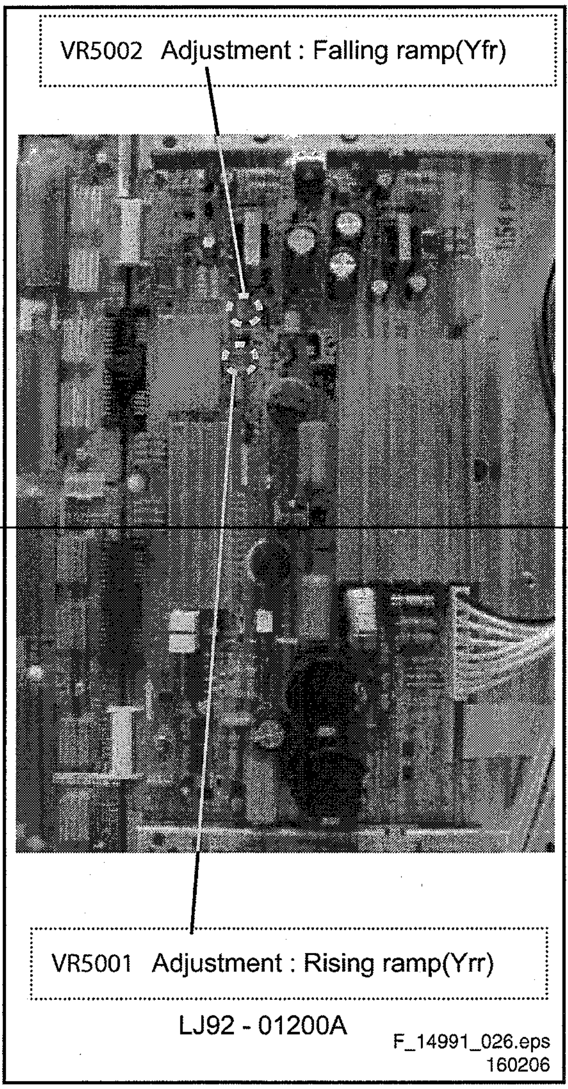
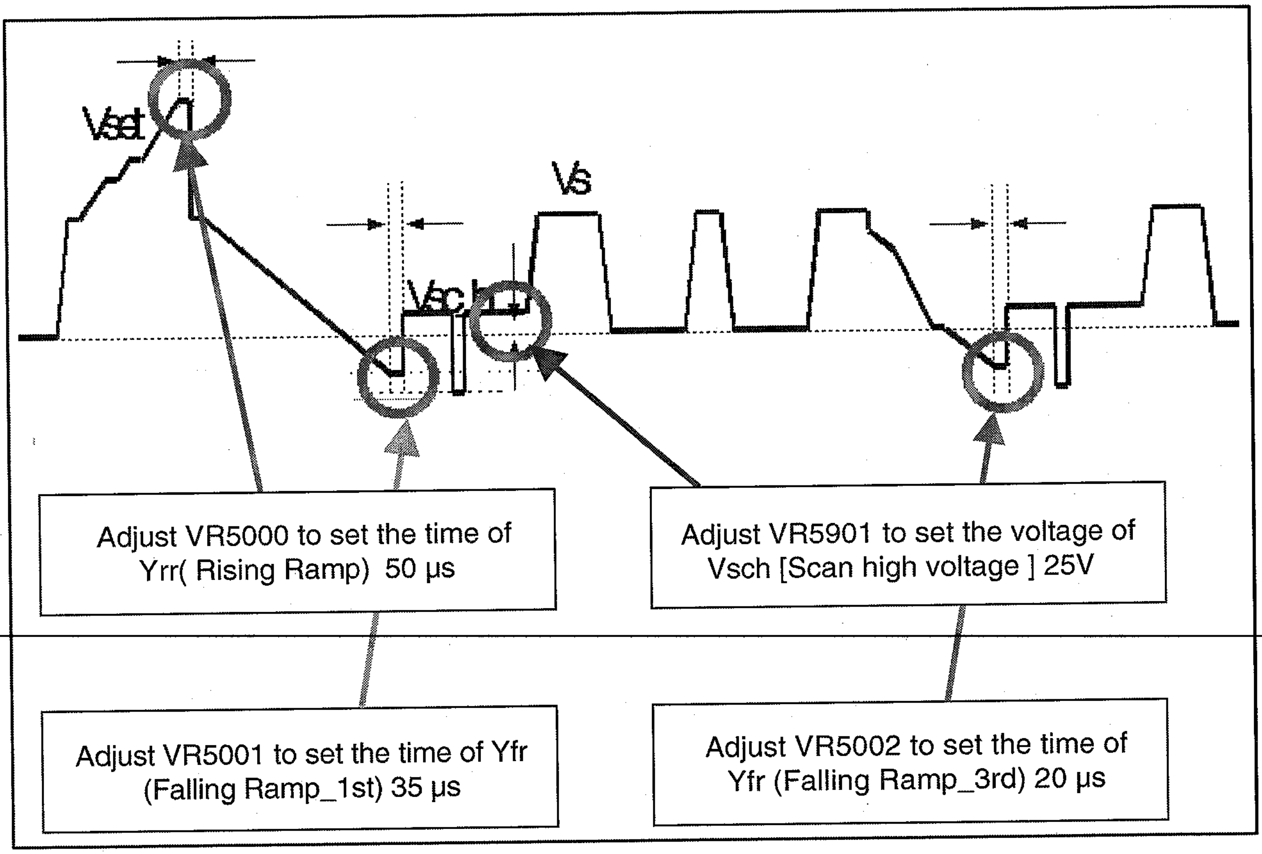

VR5002 Adjustment : Falling ramp(Yfr)
VR5001 Adjustment : Rising ramp(Yrr)
LJ92 - 01200A
F_14991_026.eps
160206

Figure 8-36 Potentiometer locations

8.7 Alignments 50" HD v3

1. Put the dipswitches on the Logic Board in the internal position to get a Full White Pattern (see Figure "DIP switch positions").
2. Adjust Vsch to 25 V by using VR5901_VSC_h (Vsc_h should be connected to "+" unit of DMM).
3. Check the waveform using Oscilloscope.
   - Triggering through V_TOGG of LOGIC Board.
   - Connect the OUT 4 Test Point at the centre of Y_buffer to other channel, and then check the first Subfield operating waveform of one TV-Field.
   - Check the waveform again after adjusting Horizontal Division. Check the Reset waveform when the V_TOGG Level is changed.
   - Set the Rising Ramp Flat Time to 50 µs by adjusting VR5000. GND maintenance section should be checked after the Vertical Division is readjusted to '2 V or 5 V'.
   - Set the Falling maintenance time to 35 µs by adjusting VR5001.
   - Change the waveform position of Oscilloscope to the 3rd Subfield and then set the Falling maintenance time to 20µs by adjusting the VR5002.
   - GND maintenance section should be checked after the Vertical Division is readjusted to '2 V or 5 V'.

Special notice: When you adjust the inclination of waveform, do check and adjustment being based on the Reset waveform of 1st Sub-field of 1st Frame and then move to 3rd Sub-field for adjusting.



Adjust VR5000 to set the time of Yrr(Rising Ramp) 50 µs

Adjust VR5901 to set the voltage of Vsch [Scan high voltage] 25V

Adjust VR5001 to set the time of Yfr (Falling Ramp_1st) 35 µs

Adjust VR5002 to set the time of Yfr (Falling Ramp_3rd) 20 µs

Figure 8-37 TCP ramp waveform inclination adjustment (Y-Board)

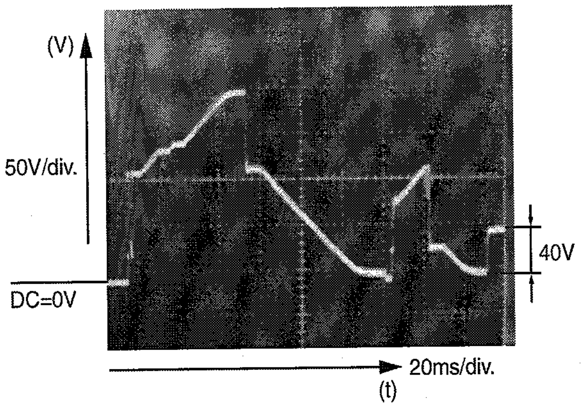


Figure 8-38 Rising ramp

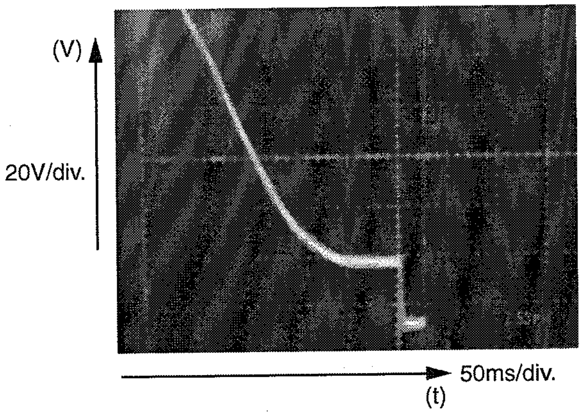
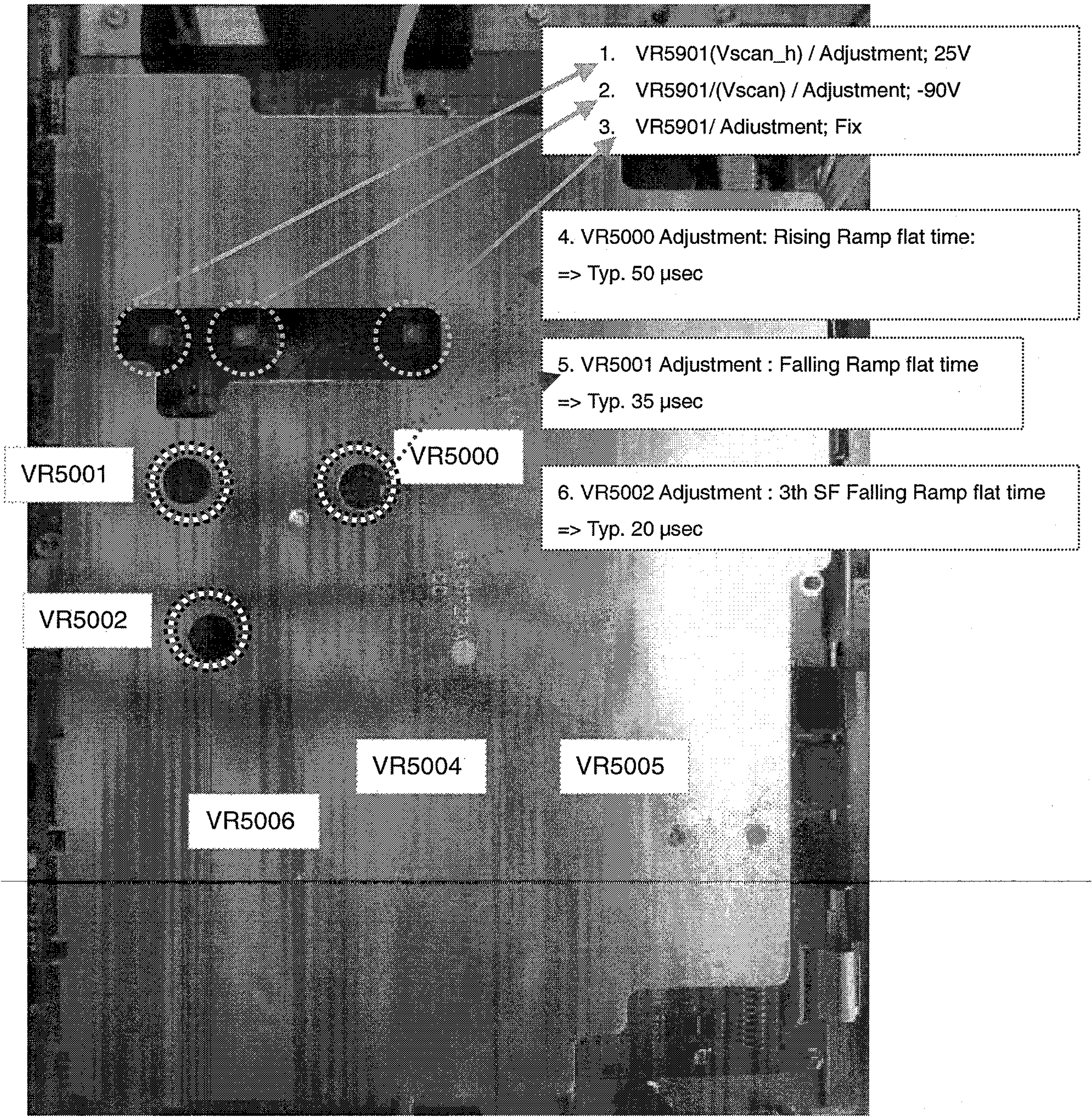


Figure 8-39 Falling ramp


VR5001
VR5000
VR5002
VR5004
VR5005
VR5006

1. VR5901(Vscan_h) / Adjustment; 25V
2. VR5901/(Vscan) / Adjustment; -90V
3. VR5901/ Adiustment; Fix

4. VR5000 Adjustment: Rising Ramp flat time:
=> Typ. 50 µsec

5. VR5001 Adjustment : Falling Ramp flat time
=> Typ. 35 µsec

6. VR5002 Adjustment : 3th SF Falling Ramp flat time
=> Typ. 20 µsec

* Pay close attention to above adjustment

Figure 8-40 Potentiometer locations

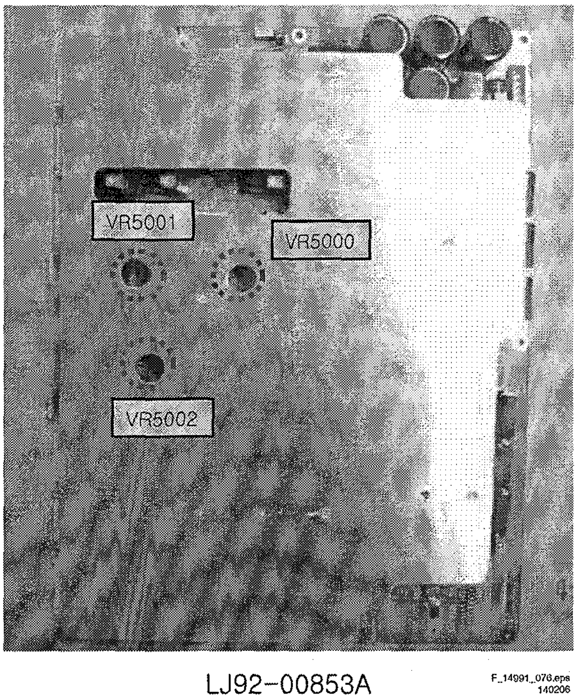

VR5001
VR5000
VR5002
LJ92-00853A
F_14991_076.eps
140206

Figure 8-41 Potentiometer locations LJ92-00853A

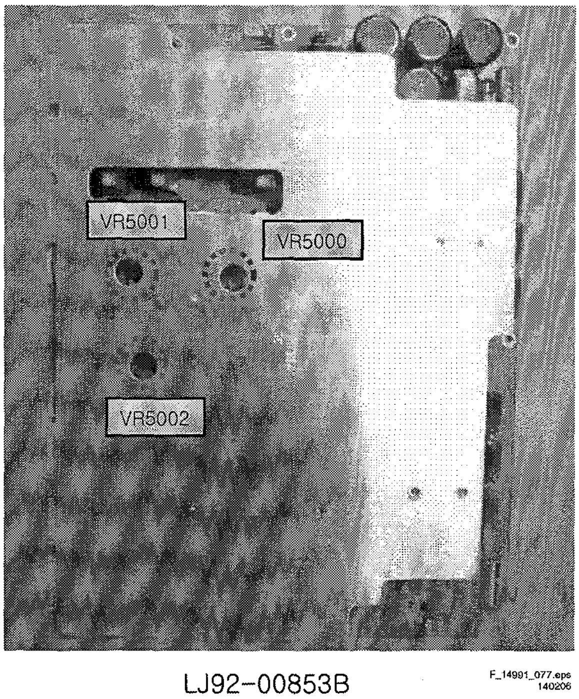

VR5001
VR5000
VR5002
LJ92-00853B
F_14991_077.eps
140206

Figure 8-42 Potentiometer locations LJ92-00853B

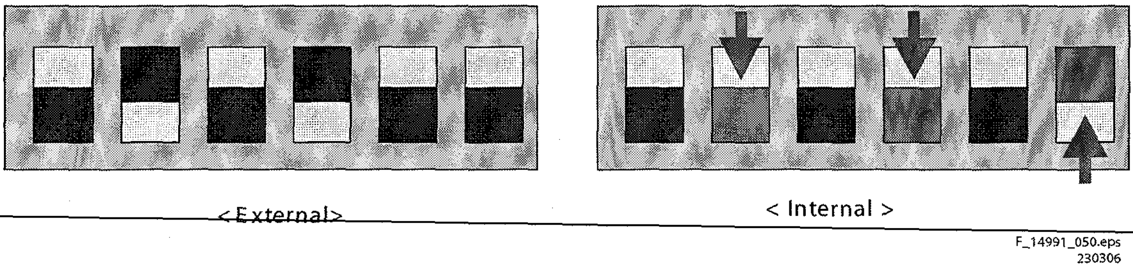
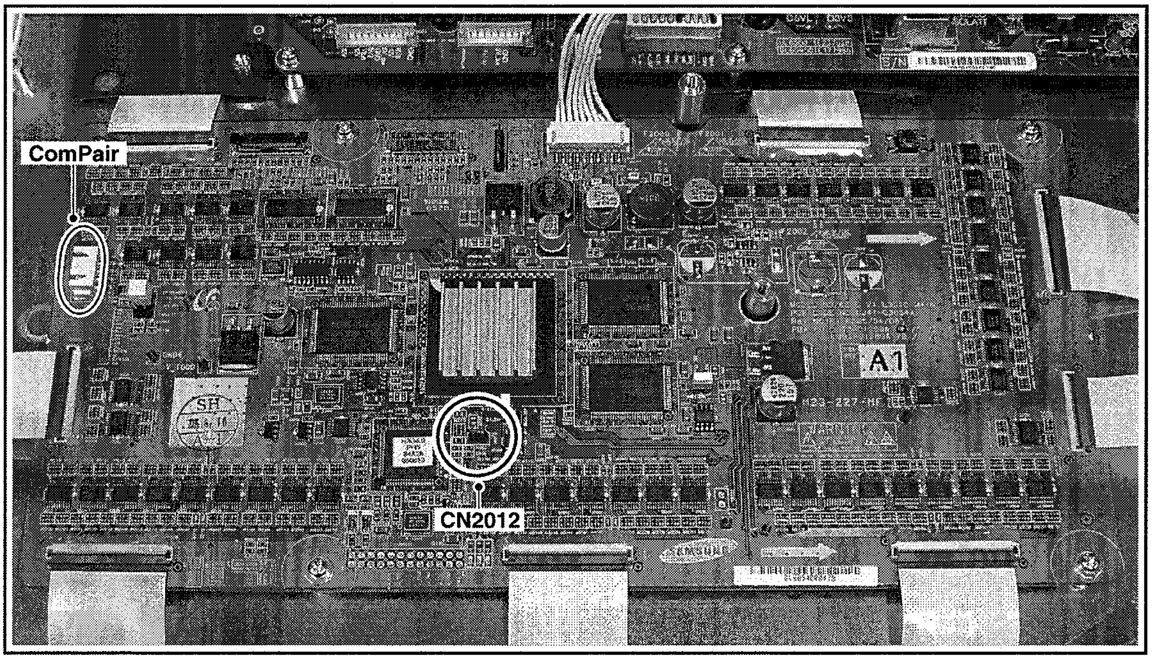

<External>
< Internal >
F_14991_050.eps
230306

Figure 8-43 DIP switch positions

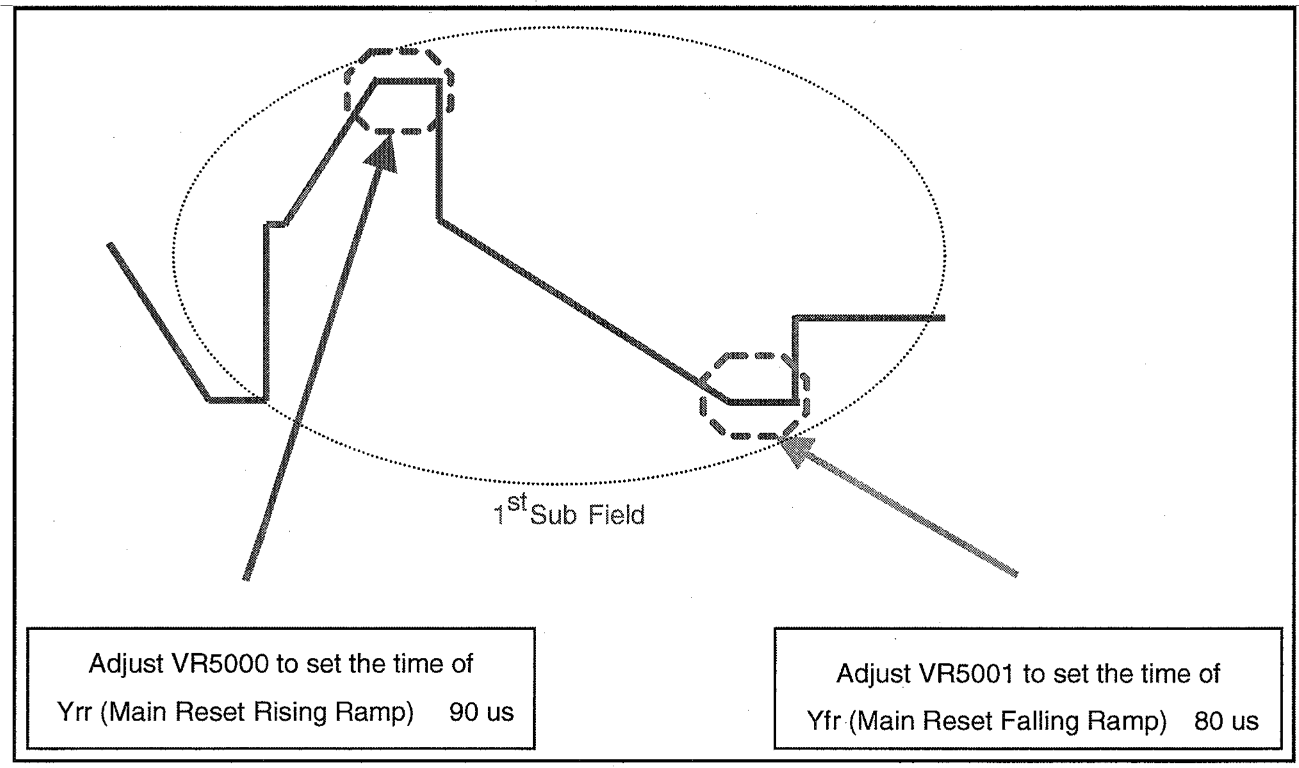
8.8 Alignments 50" HD v4

1. Get Pattern to be Full White (place jumper CN2012 on Logic Board).
2. Locate all testpoints and potentiometers of the board at hand.
   - Triggering through V_TOGG of LOGIC Board.
   - Connect the CN5511 Test Point at the Y_buffer to other channel, and then check the first Subfield operating waveform of one TV-Field.
   - Check the waveform again after adjusting Horizontal Division. Check the Reset waveform when the V_TOGG Level is changed.
   - Set the Rising Ramp Flat Time to 90 μs by adjusting VR5000.
   - Set the Falling maintenance time to 80 μs by adjusting VR5001.


ComPair
CN2012
A1

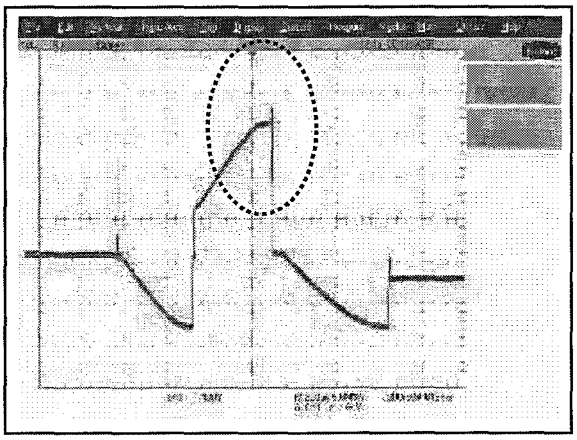
F_14991_052.eps
081105

Figure 8-44 Jumper CN2012 / ComPair connector on v4 Logic board


1st Sub Field
Adjust VR5000 to set the time of
Yrr (Main Reset Rising Ramp) 90 us
Adjust VR5001 to set the time of
Yfr (Main Reset Falling Ramp) 80 us

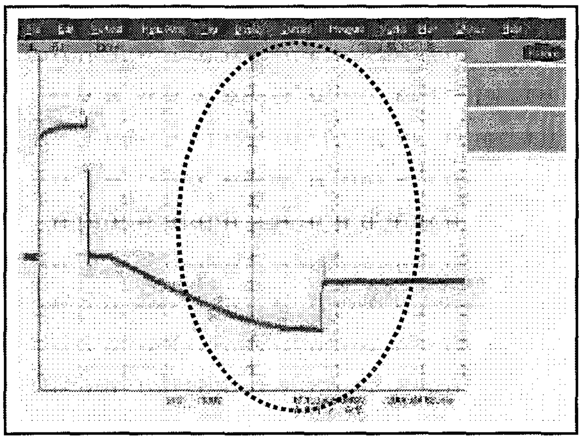
F_14991_020.eps
030805

Figure 8-45 TCP ramp waveform inclination adjustment (Y-Board)



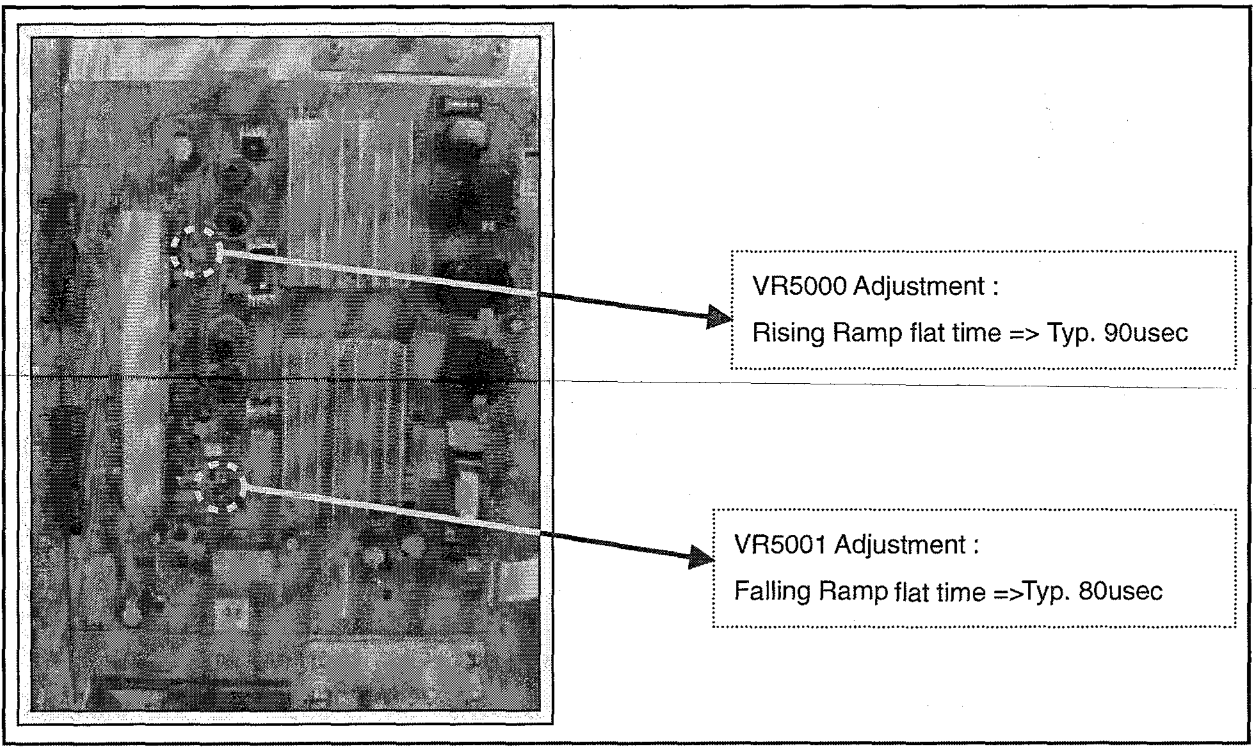
F_14991_021a.eps
030805

Figure 8-46 Rising ramp



F_14991_021b.eps
030805

Figure 8-47 Falling ramp



VR5000 Adjustment :
Rising Ramp flat time => Typ. 90usec

VR5001 Adjustment :
Falling Ramp flat time =>Typ. 80usec

F_14991_022.eps
030805

Figure 8-48 Potentiometer locations

8.9 Alignment value overview (all screens)

Table 8-1 Alignment table Y PWB

Model	Wave Form	Item	Default
37"SD v4	Rising_Ramp	VR5001	30 µs (30 ~ 40)
	Falling_Ramp_1st	VR5002	16 µs (10 ~ 20)
	Vsch	VR5000	38 V
42" SD v2	Rising_Ramp (Vset)	VR5003	10 µs
	-Vsc 1	VR5001	20 µs
	-Vsc 2	VR5002	5 µs
42" SD v3	Rising_Ramp	VR5002	10 µs
	Falling_Ramp_1st	VR5003	30 µs
	Falling_Ramp_3rd	VR5001	30 µs
	Vsch	VR5004	40 V
42" SD v4	Rising_Ramp	VR5001	60 µs
	Falling_Ramp_1st	VR5003	80 µs
42" HD v3	Rising_Ramp	VR5002	10 µs
	Falling_Ramp_1st	VR5003	20 µs
	Falling_Ramp_3rd	VR5001	10 µs
	Vsch Scan high voltage	VR5004	40 V
42" HD v4	Rising_Ramp	VR5001	15 V
	Falling_Ramp_1st	VR5002	50 µs
50" HD v3	Rising_Ramp	VR5000	50 µs
	Falling_Ramp_1st	VR5001	35 µs
	Falling_Ramp_3rd	VR5002	20 µs
	Vsch Scan high voltage	VR5901	25 V
50" HD v4	Rising_Ramp	VR5001	90 µs
	Falling_Ramp_1st	VR5003	80 µs

9. Circuit Descriptions, Abbreviation List, and IC Data Sheets

Index of this chapter:

9.1 Main function of Each Assembly
9.2 Abbreviation List
9.3 IC Data Sheets

9.1 Main function of Each Assembly

9.1.1 X Main Board

The X Main board generates a drive signal by switching the FET in synchronization with logic main board timing, and supplies the X electrode of the panel with the drive signal through the connector.

1. Maintain voltage waveforms (including ERC).
2. Generate X rising ramp signal.
3. Maintain Ve bias between Scan intervals.

9.1.2 Y Main Board

The Y Main board generates a drive signal by switching the FET in synchronization with the logic Main Board timing and sequential supplies the Y electrode of the panel with the drive signal through the scan driver IC on the Y-buffer board. This board connected to the panel's Y terminal has the following main functions.

1. Maintain voltage waveforms (including ERC).
2. Generate Y-rising Falling Ramp.
3. Maintain V scan bias.

9.1.3 Logic Main Board

The Logic Main board generates and outputs the address drive output signal and the X,Y drive signal by processing the video signals. This Board buffers the address drive output signal and feeds it to the address drive IC (COF module, video signal- X Y drive signal generation, frame memory circuit / address data rearrangement).

9.1.4 Logic Buffer (E, F)

The Logic Buffer transmits data signal and control signal.

9.1.5 Y Buffer Board (Upper, Lower)

The Y Buffer board consisting of the upper and lower boards supplies the Y-terminal with scan waveforms. The board comprises eight scan driver ICs (ST microelectronics STV 7617: 64 or 65 output pins), but four ICs for the SD class.

9.1.6 AC Noise Filter

The AC Noise filter has function for removing noise (low frequency) and blocking surge. It affects safety standards (EMC, EMI).

9.1.7 TCP (Tape Carrier Package)

The TCP applies the Va pulse to the address electrode and constitutes address discharge by the potential difference between the Va pulse and the pulse applied to the Y electrode. The TCP comprise four data driver ICs (STV7610A: 96 pins output pins). Seven TCPs are required for signal scan.

9.2 Abbreviation List

AC	Alternating Current
COF	Circuit On Foil
DC	Direct Current
ERC	Energy Recovery Circuit
ESD	Electro Static Discharge
FET	Field Effect Transistor
FFC	Flat Foil Cable
FPC	Flexible Printed Circuit
FTV	Flat TeleVision
HD	High Definition
I/O	Input/Output
IC	Integrated Circuit
LB	Logic Buffer
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signalling
PCB	Printed Circuit Board (same as PWB)
PDP	Plasma Display Panel
PSU	Power Supply Unit
PWB	Printed Wiring Board (same as PCB)
RGB	Red, Green, Blue colour space
SD	Standard Definition
SDI	Samsung Display Industry (supplier)
SMPS	Switched Mode Power Supply
SSB	Small Signal Board
SF	Sub Field
TCP	Tape Carrier Package
VR	Variable Resistor
Vsc	Scan Voltage
YBL	Y Buffer Lower board
YBU	Y Buffer Upper board
YM	Y Main board

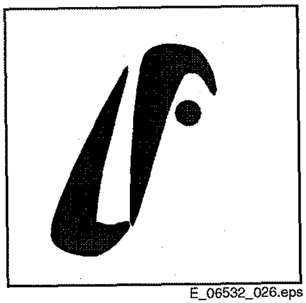
9.3 IC Data Sheets

Not applicable.

10. Spare Parts List

Notes;

- Determine the SDI part / model number of the PDP
- Find the SDI part number on the actual board to be replaced.
  SDI part number begin with "LJ92" and for the SMPS and sub SMPS the part number will begin with "LJ44".
- Find the SDI board part number in the spare parts overview.
- Find the SDI part number in this overview that matches the part number that is actually on the original board.
- Cross the SDI board part number to the philips part number.
- Order the philips part number.
- **Note:** The appearance of a leaded and lead-fraa board can be different; the colour of the PWB and also the layout of the components are sometimes different.



E_06532_026.eps
081105

Figure 10-1 Lead-free logo SDI

Table 10-1 Spare parts overview 37" SD v4

PDP type	**37" SD v4**				
PDP 12NC	**9322 217 39682 (8204 000 77261)**				**Lead Free type being compatible with Lead type PWB**
PDP model type and version	**S37SD-YD02**				
Remarks	**Lead type boards being not compatible with lead free type will not be phased out**				
Boards	**Codes for lead type PWB's**		**Codes for lead-free type PWB's**		
Logic-Buffer (E)	LJ92-00976A	9965 000 26187	LJ92-01138B	9965 000 32616	N
Logic-Buffer (F)	LJ92-00977A	9965 000 26188	LJ92-01139B	9965 000 32617	N
Logic-Buffer (G)	LJ92-01002A	9965 000 26189	LJ92-01140B	9965 000 32618	N
Logic-Buffer (H)	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-
Y-Buffer (up)	LJ92-01022A	9965 000 26190	LJ92-01147A	9965 000 32619	N
Y-Buffer (down)	-	-	-	-	-
Logic-Board	LJ92-01056A **(See Kit 1 Note)** LJ92-01145A **(See Kit 2 Note)**	9965 000 26191	LJ92-01257A	9965 000 29322	N
SUBL	-	-	-	-	-
SUBR	-	-	-	-	-
~~X-Board~~	~~LJ92-01020A~~	~~9965 000 26192~~	~~LJ92-01268A~~	~~9965 000 32620~~	~~N~~
Y-Board	LJ92-01021A	9965 000 26193	LJ92-01149B	9965 000 32621	N
SMPS (PSU)	LJ44-00084A	9965 000 26194	LJ44-00084B	9965 000 32622	Y
SUB PSU	LJ44-00075A	9965 000 25131	LJ44-00075B	9965 000 32623	Y
		Kit 1	LJ93-00205A	9965 000 33796	
		Kit 2	LJ93-00204A	9965 000 33797	

Note:
Kit 1: 37" FCR kit concists of 4 boards (Logic + Y-main + Y and E buffer)
reference Symptom Cure information TV-05/0006
CORRECTION XI: PDP with "Lead" boards and use of Logic board (LJ92-01056A):
Replace the Logic board, the Y-Main board, the Y-buffer board, and the Logic buffer E board together.
These four boards are available in Service Kit number 1 (with order code 9965 000 33796 (LJ93-00205A)).

The content of Service Kit number 1 is:

* Logic main board	9965 000 29322	(LJ92-01257A).
* Y-Main board	9965 000 32621	(LJ92-01149B).
* Y-Buffer board	9965 000 32619	(LJ92-01147A).
* Logic-Buffer E	9965 000 32616	(LJ92-01138B).

Note:
FCR Kit: = False contouring reduction kit

Note:
Kit 2: 37" FCR kit concists of 2 boards (logic + Y-main)
reference Symptom Cure information TV-05/0006
CORRECTION XI
PDP with "Lead-free" boards and use of Logic board (LJ92-01145A):
Replace the Logic board and the Y-Main board together. These two boards are available in Service Kit number 2 (with order code 9965 000 33797 (LJ93-00204A)).

The content of Service Kit number 2 is:

* Logic main board	9965 000 29322	(LJ92-01257A).
* Y-Main board	9965 000 32621	(LJ92-01149B).

3) PDP with "Lead-free" boards and use of Logic board (LJ92-01257A):
In case this PDP has a defective board, replace this defective board only

Table 10-2 Spare parts overview 42" SD v2

PDP type	**42"SDv2**	
PDP model 12NC	**9322 195 45682**	
PDP model type and version	**S42SD-YD06**	
Remarks	**Codes for lead type PWBs (this model has been produced *with leaded type PWB's only)***	
Boards	**PWB Codes**	
Logic-Buffer (E)	LJ92-00632A	9965 000 17726
Logic-Buffer (F)	LJ92-00633A	9965 000 17725
Logic-Buffer (G)	LJ92-00634A	9965 000 17724
Logic-Buffer (H)	-	-
Logic-Buffer (I)	-	-
Logic-Buffer (J)	-	-
Y-Buffer (up)	LJ92-00751A	9965 000 17727
Y-Buffer (down)	LJ92-00750A	9965 000 17728
Logic-Board	LJ92-00818A	9965 000 17729
SUBL	-	-
SUBR	-	-
X-Board	LJ92-00998A	9965 000 17720
Y-Board	LJ92-00999A	9965 000 17731
SMPS (PSU)	LJ44-00049A	9965 000 17730
SUB PSU	-	-

Table 10-3 Spare parts overview 42" SD v3

PDP type	**42" SD v3**				**Lead Free type *being compatible* with Lead type PWB**
PDP model 12NC	**9322 215 27682**				
PDP model type and version	**S42SD-YD05**				
Remarks	**Lead type boards being phased out**				
Boards	**Codes for leaded type PWBs**		**Codes for lead-free type PWBs**		
Logic-Buffer (E)	LJ92-00811A	9965 000 25109	LJ92-00811B	9965 000 32624	Y
Logic-Buffer (F)	LJ92-00812A	9965 000 25110	LJ92-00812B	9965 000 32625	Y
Logic-Buffer (G)	LJ92-00813A	9965 000 25111	LJ92-00813B	9965 000 32626	Y
Logic-Buffer (H)	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-
Y-Buffer (up)	LJ92-00796A	9965 000 25112	LJ92-01285A	9965 000 32376	Y
Y-Buffer (down)	LJ92-00797A	9965 000 25113	LJ92-01286A	9965 000 32377	Y
Logic-Board	LJ92-00975D	9965 000 25114	LJ92-01247D	9965 000 32378	N (tbd)
SUBL	-	-	-	-	-
SUBR	-	-	-	-	-
X-Board	LJ92-00943A	9965 000 25115	LJ92-01283A	9965 000 32627	Y
Y-Board	LJ92-00944B	9965 000 25116	LJ92-01284A	9965 000 32379	Y
SMPS (PSU)	LJ44- 000 58A	9965 000 25108	LJ44-00058B	9965 000 32638	Y
SUB PSU	LJ44- 000 75A	9965 000 25131	LJ44-00075B	9965 000 32623	Y

Table 10-4 Spare parts overview 42" SD v4 (Part 1)

PDP type	**42" SD v4**				**Boards from PP42SD015A and S42SD-YD07 (*) being *compatible***
PDP model 12NC	**9322 226 37682**				
PDP model type and version	**S42SD-YD07 (*)**		**S42SD-YD07 (PP42SD015A)**		
Remarks	**No supply of new SMPS LJ44-00092B. *Compatibility with LJ44-00101C + cable: tdb (15/2)***		**Version number used by SDI:PP42SD015B(SMPS Rev.0.55) New SMPS supply:LJ44-00101C + cables. Service *information: tbd***		
Logic-Buffer (E)	LJ92-01026A	9965 000 29205	LJ92-01026A	9965 000 29205	Y
Logic-Buffer (F)	LJ92-01027A	9965 000 29206	LJ92-01027A	9965 000 29206	Y
Logic-Buffer (G)	-	-	-	-	-
Logic-Buffer (H)	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-
Y-Buffer (up)	LJ92-01031A	9965 000 29207	LJ92-01031A	9965 000 29207	Y
Y-Buffer (down)	LJ92-01032A	9965 000 29208	LJ92-01032A	9965 000 29208	Y
Logic-Board	LJ92-01274D	9966 000 30042	LJ92-01274D	9966 000 30042	Y
SUBL	-	-	-	-	-
SUBR	-	-	-	-	-
X-Board	LJ92-01029A	9965 000 29204	LJ92-01336A	9965 000 32628	Y
Y-Board	LJ92-01030A	9965 000 29209	LJ92-01337A	9965 000 32629	Y
SMPS (PSU)	LJ44-00092B	9965 000 29210	LJ44-00101A	9965 000 29210	N (tdb)
SUB PSU	-	-	-	-	-

Table 10-5 Spare parts overview 42" SD v4 (Part 2)

PDP type	42" SD v4					Service Information 932223381682 being backwards compatible tbd
PDP model 12NC	9322 226 96682			9322 233 81682		
PDP model type and version	S42SD-YD07 (PP42SD015B)			S42SD-YD07 (PP42SD015F)		PWB's from PP42SD015B and PP42SD015F being compatible
Remarks	Version number used by SDI:PP42SD015B(SMPS Rev.0.55) New SMPS supply:LJ44-00101C + cables. Service information: tbd		PWB's from PP42SD015B and PP42SD015A being compatible	Version number used by SDI: PP42SD015F (SMPS Rev.0.7)		
Logic-Buffer (E)	LJ92-01026A	9965 000 29205	Y	LJ92-01026A	9965 000 29205	Y
Logic-Buffer (F)	LJ92-01027A	9965 000 29206	Y	LJ92-01027A	9965 000 29206	Y
Logic-Buffer (G)	-	-	-	-	-	-
Logic-Buffer (H)	-	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-	-
Y-Buffer (up)	LJ92-01031A	9965 000 29207	Y	LJ92-01031A	9965 000 29207	Y
Y-Buffer (down)	LJ92-01032A	9965 000 29208	Y	LJ92-01032A	9965 000 29208	Y
Logic-Board	LJ92-01274D	9966 000 30042	Y	LJ92-01274D	9966 000 30042	Y
SUBL	-	-	-	-	-	-
SUBR	-	-	-	-	-	-
X-Board	LJ92-01336A	9965 000 32628	Y	LJ92-01336A	9965 000 32628	Y
Y-Board	LJ92-01337A	9965 000 32629	Y	LJ92-01337A	9965 000 32629	Y
SMPS (PSU)	LJ44-00101B	9965 000 32630	N	LJ44-00101C	9965 000 33880	Y
SUB PSU	-	-	-	-	-	-

Table 10-6 Spare parts overview 42" HD v3

PDP type	42" HD v3				Lead Free type being compatible with Lead type PWB
PDP model 12NC	9322 215 25682				
PDP model type and version	S42AX-XD02				
Remarks	Lead type boards being phased out				
Boards	Codes for leaded type PWBs		Codes for lead-free type PWBs		
Logic-Buffer (E)	LJ92-00895A	9965 000 25101	LJ92-01264A	9965 000 32631	Y
Logic-Buffer (F)	LJ92-00896A	9965 000 25102	LJ92-01265A	9965 000 32632	Y
Logic-Buffer (G)	-	-	-	-	-
Logic-Buffer (H)	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-
Y-Buffer (up)	LJ92-00993A	9965 000 25103	LJ92-00993B	9965 000 32633	Y
Y-Buffer (down)	LJ92-00994A	9965 000 25104	LJ92-00994B	9965 000 32634	Y
Logic-Board	LJ92-00990E	9965 000 25105	LJ92-01221C	9965 000 32635	Y
SUBL	-	-	-	-	-
SUBR	-	-	-	-	-
X-Board	LJ92-00980A	9965 000 25106	LJ92-00980B	9965 000 32636	Y
Y-Board	LJ92-00981A	9965 000 25107	LJ92-00981B	9965 000 32637	Y
SMPS (PSU)	LJ44-00058A	9965 000 25108	LJ44-00058B	9965 000 32638	Y
SUB PSU	LJ44-00075A	9965 000 25131	LJ44-00075B	9965 000 32623	Y

Table 10-7 Spare parts overview 42" HD v4 (Part 1)

PDP type	42" HD v4				Boards from S42AX-YD01(*) and PP42AX-007A being Compatible
PDP model 12NC	8204 000 78191		9322 225 38682		
PDP model type and version	S42AX-YD01 (*)		S42AX-YD01 (PP42AX-007A)		
Remarks	SMPS LJ44-00092A being phased out supply:LJ44-00101C + cables. Service information: tbd		(SMPS Rev.0.55) New SMPS supply:LJ44-00101C + cables. Service information: tbd		
Logic-Buffer (E)	LJ92-01054A	9965 000 29197	LJ92-01054A	9965 000 29197	Y
Logic-Buffer (F)	LJ92-01055A	9965 000 29198	LJ92-01055A	9965 000 29198	Y
Logic-Buffer (G)	-	-	-	-	-
Logic-Buffer (H)	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-
Y-Buffer (up)	LJ92-01117A	9965 000 29199	LJ92-01202A	9965 000 32639	Y
Y-Buffer (down)	LJ92-01118A	9965 000 29200	LJ92-01203A	9965 000 32640	Y
Logic-Board	LJ92-01053A	9965 000 29203	LJ92-01270B	9965 000 32641	Y
SUBL	-	-	-	-	-
SUBR	-	-	-	-	-
X-Board	LJ92-01115A	9965 000 29196	LJ92-01199A	9965 000 32642	Y
Y-Board	LJ92-01200A	9965 000 32643	LJ92-01200A	9965 000 32643	Y
SMPS (PSU)	LJ44-00092A	9965 000 29202	LJ44-00101A	9965 000 29210	N
SUB PSU	-	-	-	-	-

Table 10-8 Spare parts overview 42" HD v4 (Part 2)

PDP type	**42" HD v4**					**Service Information 9322 233 80682 being backwards compatible tbd**
PDP model 12NC	**9322 226 95682**			**9322 233 80682**		
PDP model type and version	**S42AX-YD01 (PP42AX-008A)**		**PWB's from PP42AX-007A and PP42AX-008A being Compatible**	**S42AX-YD01 (PP42AX-008B)**		**PWB's from PP42AX-008A and PP42AX-008B being compatible**
Remarks	**(SMPS Rev.0.65) New SMPS supply:LJ44-*00101C + cables. Service information: tbd***			**(SMPS Rev.0.55) New SMPS supply:LJ44-00101C + cables. Service information: tbd**		
Logic-Buffer (E)	LJ92-01054A	9965 000 29197	Y	LJ92-01054A	9965 000 29197	Y
Logic-Buffer (F)	LJ92-01055A	9965 000 29198	Y	LJ92-01055A	9965 000 29198	Y
Logic-Buffer (G)	-	-	-	-	-	-
Logic-Buffer (H)	-	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-	-
Y-Buffer (up)	LJ92-01202A	9965 000 32639	Y	LJ92-01202A	9965 000 32639	Y
Y-Buffer (down)	LJ92-01203A	9965 000 32640	Y	LJ92-01203A	9965 000 32640	Y
Logic-Board	LJ92-01270B	9965 000 32641	Y	LJ92-01270B	9965 000 32641	Y
SUBL	-	-	-	-	-	-
SUBR	-	-	-	-	-	-
X-Board	LJ92-01199A	9965 000 32642	Y	LJ92-01199A	9965 000 32642	Y
Y-Board	LJ92-01200A	9965 000 32643	Y	LJ92-01200A	9965 000 32643	Y
SMPS (PSU)	LJ44-00101B	9965 000 32630	N	LJ44-00101C	9965 000 33880	Y
SUB PSU	-	-	-	-	-	-

Table 10-9 Spare parts overview 50" HD v3

PDP type	**50" HD v3**				
PDP model 12NC	**9322 215 26682**				
PDP model type and version	**S50HW-XD03 (PP50HW004C)**				
Remarks	**Lead type boards being phased out**				**Lead Free type being compatible with Lead type PWB**
Boards	**Codes for leaded type PWBs**		**Codes for lead-free typePWBs**		
Logic-Buffer (E)	LJ92-00917A	9965 000 25117	LJ92-00917B	9965 000 32614	Y
Logic-Buffer (F)	LJ92-00918A	9965 000 25118	LJ92-00918B	9965 000 32615	Y
Logic-Buffer (G)	LJ92-00919A	9965 000 25119	LJ92-00919B	9965 000 32646	Y
Logic-Buffer (H)	LJ92-00920A	9965 000 25120	LJ92-00920B	9965 000 32647	Y
Logic-Buffer (I)	LJ92-00921A	9965 000 25121	LJ92-00921B	9965 000 32648	Y
Logic-Buffer (J)	LJ92-00922A	9965 000 25122	LJ92-00922B	9965 000 32649	Y
Y-Buffer (up)	LJ92-00880A	9965 000 25123	LJ92-00880B	9965 000 32650	Y
Y-*Buffer (down)*	LJ92-00881A	9965 000 25124	LJ92-00881B	9965 000 32651	Y
Logic-Board	LJ92-00949C	9965 000 25125	LJ92-01224B	9965 000 32652	Y
SUBL	LJ92-00923A	9965 000 25126	LJ92-00923B	9965 000 32653	Y
SUBR	LJ92-00959A	9965 000 25127	LJ92-00959B	9965 000 32654	Y
X-Board	LJ92-00852A	9965 000 25128	LJ92-00852B	9965 000 32655	Y
Y-Board	LJ92-00853A	9965 000 25129	LJ92-00853B	9965 000 32656	Y
SMPS (PSU)	LJ44-000 65A	9965 000 25130	LJ44-00065B	9965 000 32657	Y
SUB PSU	LJ44-000 99A	9965 000 26195	LJ44-00099B	9965 000 32658	Y

Table 10-10 Spare parts overview 50” HD v4 (Part 1)

PDP type	**50" HD v4**				
PDP model 12NC	**9322 226 54682**		**9322 226 97682**		
PDP model type and version	**S50HW-XD04 (PP50HW-005A)**		**S50HW-XD04 (PP50HW-005B)**		**PWB's from PP50HW-005A and PP50HW-005B being compatible**
Remarks	**Codes for PWBs from 932222654682 PP50H-005A** **New SMPS supply:LJ44-00108C + cables.** **Service information: tbd**		**Codes for PWBs from 932222697682 PP50H-005B** **New SMPS supply:LJ44-00108C + cables.** **Service information: tbd**		
Logic-Buffer (E)	LJ92-01103A	9965 000 30025	LJ92-01103A	9965 000 30025	Y
Logic-Buffer (F)	LJ92-01104A	9965 000 30026	LJ92-01104A	9965 000 30026	Y
Logic-Buffer (G)	LJ92-01105A	9965 000 30027	LJ92-01105A	9965 000 30027	Y
Logic-Buffer (H)	-	-	-	-	-
Logic-Buffer (I)	-	-	-	-	-
Logic-Buffer (J)	-	-	-	-	-
Y-Buffer (up)	LJ92-01047A	9965 000 30028	LJ92-01047A	9965 000 30028	Y
Y-Buffer (down)	LJ92-01048A	9965 000 30029	LJ92-01048A	9965 000 30029	Y
Logic-Board	LJ92-01269B	9965 000 30032	LJ92-01269B	9965 000 30032	Y
SUBL	-	-	-	-	-
SUBR	-	-	-	-	-
X-Board	LJ92-01045A	9965 000 30024	LJ92-01045A	9965 000 30024	Y
Y-Board	LJ92-01046A	9965 000 30030	LJ92-01046A	9965 000 30030	Y
SMPS (PSU)	LJ44-00108A	9965 000 33390	LJ44-00108B	9965 000 30031	N
SUB PSU	-	-	-	-	-

Table 10-11 Spare parts overview 50” HD v4 (Part 2)

PDP type	**50" HD v4**		**Service information: 932223379682 being backwards compatible: tdb**
PDP model 12NC	**9322 233 79682**		
PDP model type and version	**S50HW-XD04 (PP50HW-005B)**		**PWB's from PP50HW-005B and PP50HW-005E being compatible**
Remarks	**Codes for PWBs from 932223379682 PP50H-005E**		
Logic-Buffer (E)	LJ92-01103A	9965 000 30025	Y
Logic-Buffer (F)	LJ92-01104A	9965 000 30026	Y
Logic-Buffer (G)	LJ92-01105A	9965 000 30027	-
Logic-Buffer (H)	-	-	-
Logic-Buffer (I)	-	-	-
Logic-Buffer (J)	-	-	-
Y-Buffer (up)	LJ92-01047A	9965 000 30028	Y
Y-Buffer (down)	LJ92-01048A	9965 000 30029	Y
Logic-Board	LJ92-01269B	9965 000 30032	Y
SUBL	-	-	-
SUBR	-	-	-
X-Board	LJ92-01045A	9965 000 30024	Y
Y-Board	LJ92-01046A	9965 000 30030	Y
SMPS (PSU)	LJ44-00108C	9965 000 33879	Y
SUB PSU	-	-	-

Note: All 42- and 50-inch v4 panels are lead-free. Differences in table above are related to the SMPS (PSU).

11. Revision List

Manual xxxx xxx xxxx.0
- First release.

Manual xxxx xxx xxxx.1
- **General:** Update of whole manual to the latest publication standards and information.
- **37" SD v4:** Errors corrected, and info updated.
- **42" SD v2:** Errors corrected, and info updated.
- **42" SD v3:** Errors corrected, and info updated.
- **42" SD v4:** New.
- **42" HD v3:** Errors corrected, and info updated.
- **42" HD v4:** New.
- **50" HD v3:** Errors corrected, and info updated.
- **50" HD v4:** New.

Manual xxxx xxx xxxx.2
- SMPS layouts and voltages updated
- Alignments updated
- Parts list updated

Manual xxxx xxx xxxx.3
- **General:** Correction of some minor errors.
- **Chapter 8, Alignments:** Errors corrected, and info updated.

Colour Television **Module**

SDI PDP 2K6

S42SD-YD09 (42-inch SD, v5)
S42AX-YD02 (42-inch HD, w1)
S50HW-YD01 (50-inch HD, w1)
S63HW-XD05 (63-inch HD, v4)

Service
Service
Service

Service Manual

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PHILIPS

1. Technical Specifications, Connections, and Chassis Overview

Index of this chapter:

1.1 PDP Overviews
1.2 Serial Numbers
1.3 Chassis Overviews

Notes:

- Figures can deviate due to the different model executions.
- Specifications are indicative (subject to change).

1.1 PDP Overviews

Table 1-1 PDP overview

	PDP Type / Version	Model Name	H x V Pixel
1	42" SD v5	S42SD-YD09	852 x 480
2	42" HD w1	S42AX-YD02	1024 x 768
3	50" HD w1	S50HW-YD01	1366 x 768
4	63" HD v4	S63HW-XD05	1366 x 768

Table 1-2 PDP vs Chassis overview

Display type	Model #	Chassis	Chassis Manual #
42" SD v5	42PF5521D/10	LC4.41E AB	3122 785 16230
42" SD v5	42PF5521D/12	LC4.41E AB	3122 785 16230
42" HD w1	42PF9431D/37	BJ2.5U PA	3122 785 15930
42" HD w1	42PF9631D/37	BJ2.4U PA	3122 785 15920
50" HD w1	50PF9631D/37	BJ2.4U PA	3122 785 15920
50" HD w1	50PF9731D/37	BJ2.4U PA	3122 785 15920
63" HD v4	63PF9631D/37	BJ3.0U PA	3122 785 16460

In above table the link is given between the SDI Plasma Display Panel and the Philips TV chassis (incl. chassis manual no.).

1.1.1 42" SD v5

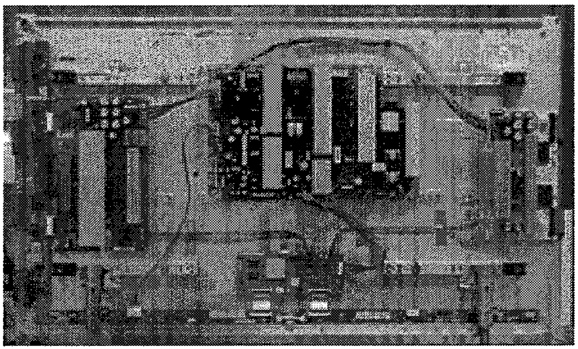

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Figure 1-1 Rear view of plasma panel (42" SD v5)

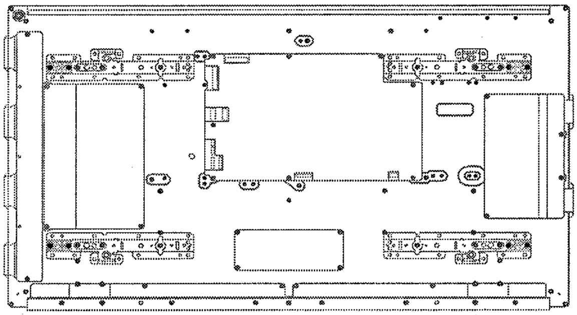

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Figure 1-2 Location of mounting screws (42" SD v5)

NOTE: screw torque 9.5 ± 0.5 kgf.cm

No	Item	Specification 42" SD v5	
1	Pixel	852 (H) x 480 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	2556 (H) x 480 (V)	
3	Pixel Pitch	1.095 (H) mm x 1.110 (V) mm	
4	Cell Pitch	R	0.365 (H) mm x 1.110 (V) mm
		G	0.365 (H) mm x 1.110 (V) mm
		B	0.365 (H) mm x 1.110 (V) mm
5	Display size	932.940 (H) x 532.800 (V) mm	
6	Screen size	Diagonal 42" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	16.77 million colours (8-bit)	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 54 (D) mm	
11	Weight	1 Module	About 15.4 kg
14	Vertical frequency and Video/Logic Interface	60 Hz/ 50 Hz, LVDS	

1.1.2 42" HD w1

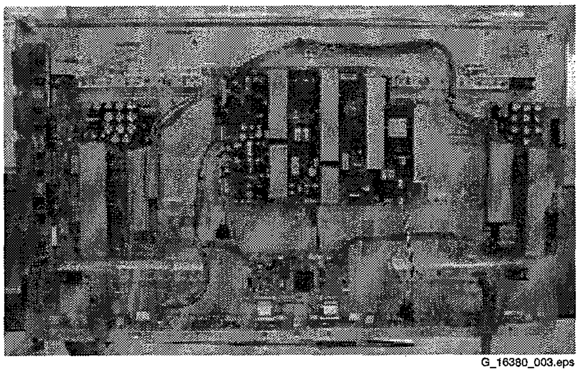

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Figure 1-3 Rear view of plasma panel (42" HD w1)

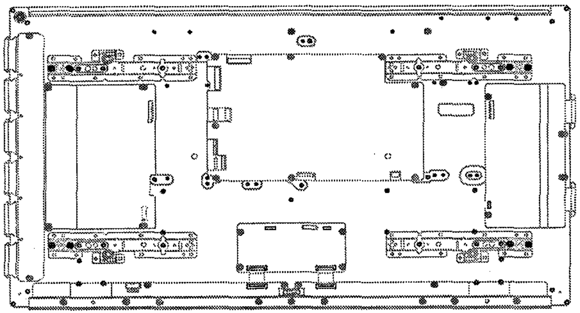

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Figure 1-4 Location of mounting screws (42" HD w1)

NOTE: screw torque 9.5 ± 0.5 kgf.cm

No	Item	Specification 42" HD w1	
1	Pixel	1,024 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	3072 (H) x 768 (V)	
3	Pixel Pitch	0.912mm (H) x 0.693mm (V)	
4	Cell Pitch	R	Horizontal 0.304 mm Vertical 0.693 mm
		G	Horizontal 0.304 mm Vertical 0.693 mm
		B	Horizontal 0.304 mm Vertical 0.693 mm
5	Display size	933.89 (H) x 532.22 (V) mm	
6	Screen size	Diagonal 42" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	1073.7 million colours (10-bit)	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 54 (D) mm	
11	Weight	1 Module	About 16.8 kg
12	Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.3 50" HD w1

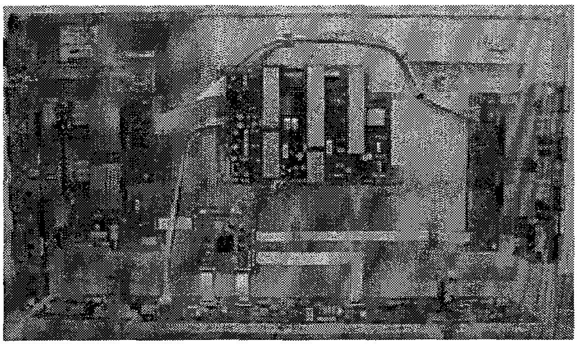

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Figure 1-5 Rear view of plasma panel (50" HD w1)

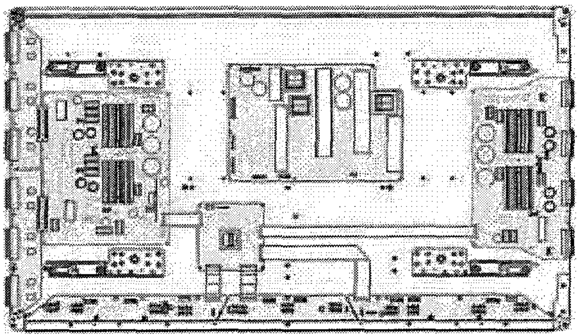

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Figure 1-6 Location of mounting screws (50" HD w1)

NOTE: screw torque 9.5 ± 0.5 kgf.cm

No	Item	Specification 50" HD w1	
1	Pixel	1366 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	4,098 (H) x 768 (V) cells	
3	Pixel Pitch	0.810 mm (H) x 0.810 mm (V)	
4	Cell Pitch	R	Horizontal 0.270 mm Vertical 0.810 mm
		G	Horizontal 0.270 mm Vertical 0.810 mm
		B	Horizontal 0.270 mm Vertical 0.810 mm
5	Display size	1106.46 mm (H) x 622.08 mm (H)	
6	Screen size	Diagonal 50" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	549.75 billion colours (13-bit)	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	1175 (W) x 678.5 (H) x 63.8 (D) mm	
11	Weight	Module 1	About 18.0 kg
12	Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.1.4 63" HD v4

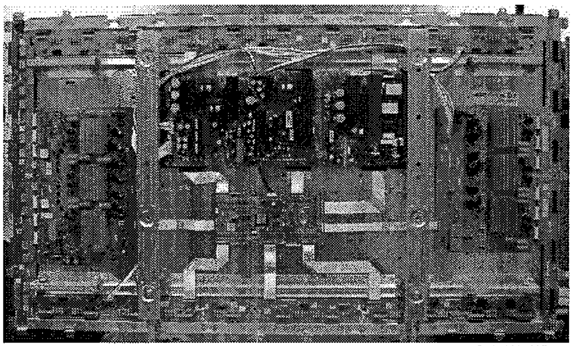

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Figure 1-7 Rear view of plasma panel (63" HD v4)

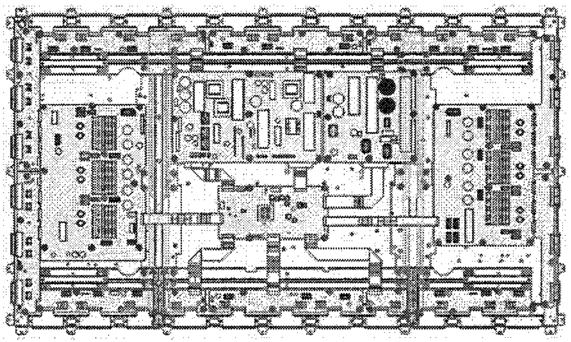

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Figure 1-8 Location of mounting screws (63" HD v4)

NOTE: screw torque 9.5 ± 0.5 kgf.cm

No	Item	Specification 63" HD v4	
1	Pixel	1366 (H) x 768 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	4,098 (H) x 768 (V) cells	
3	Pixel Pitch	1.02 mm (H) x 1.02 mm (V)	
4	Cell Pitch	R	Horizontal 0.34 mm Vertical 1.02 mm
		G	Horizontal 0.34 mm Vertical 1.02 mm
		B	Horizontal 0.34 mm Vertical 1.02 mm
5	Display size	1393.3 mm (H) x 783.4 mm (H)	
6	Screen size	Diagonal 63" Colour Plasma Display Module	
7	Screen aspect	16:9	
8	Display colour	1073.7 million colours (13-bit)	
9	Viewing angle	Over 160 deg (angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	approx. 1680 (W) x 875 (H) x 750 (D) mm	
11	Weight	Module 3	About 44.0 kg
12	Vertical frequency Video/Logic Interface	60/50 Hz, LVDS	

1.2 Serial Numbers

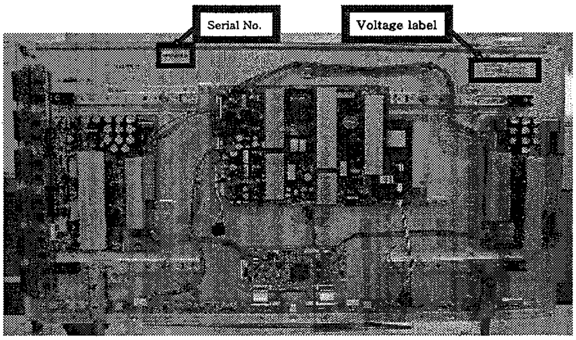
Serial No.
Voltage label

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Figure 1-9 Location of the serial number

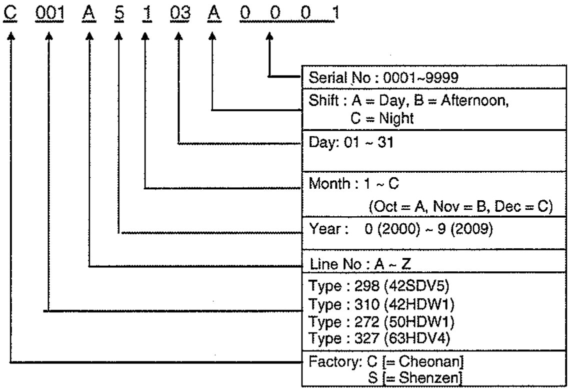
C 001 A 5 1 03 A 0 0 0 1
Serial No : 0001~9999
Shift : A = Day, B = Afternoon, C = Night
Day: 01 ~ 31
Month : 1 ~ C (Oct = A, Nov = B, Dec = C)
Year : 0 (2000) ~ 9 (2009)
Line No : A ~ Z
Type : 298 (42SDV5)
Type : 310 (42HDW1)
Type : 272 (50HDW1)
Type : 327 (63HDV4)
Factory: C [= Cheonan]
S [= Shenzen]

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Figure 1-10 Explanation of the serial number

1.3 Chassis Overviews

1.3.1 42" SD v5

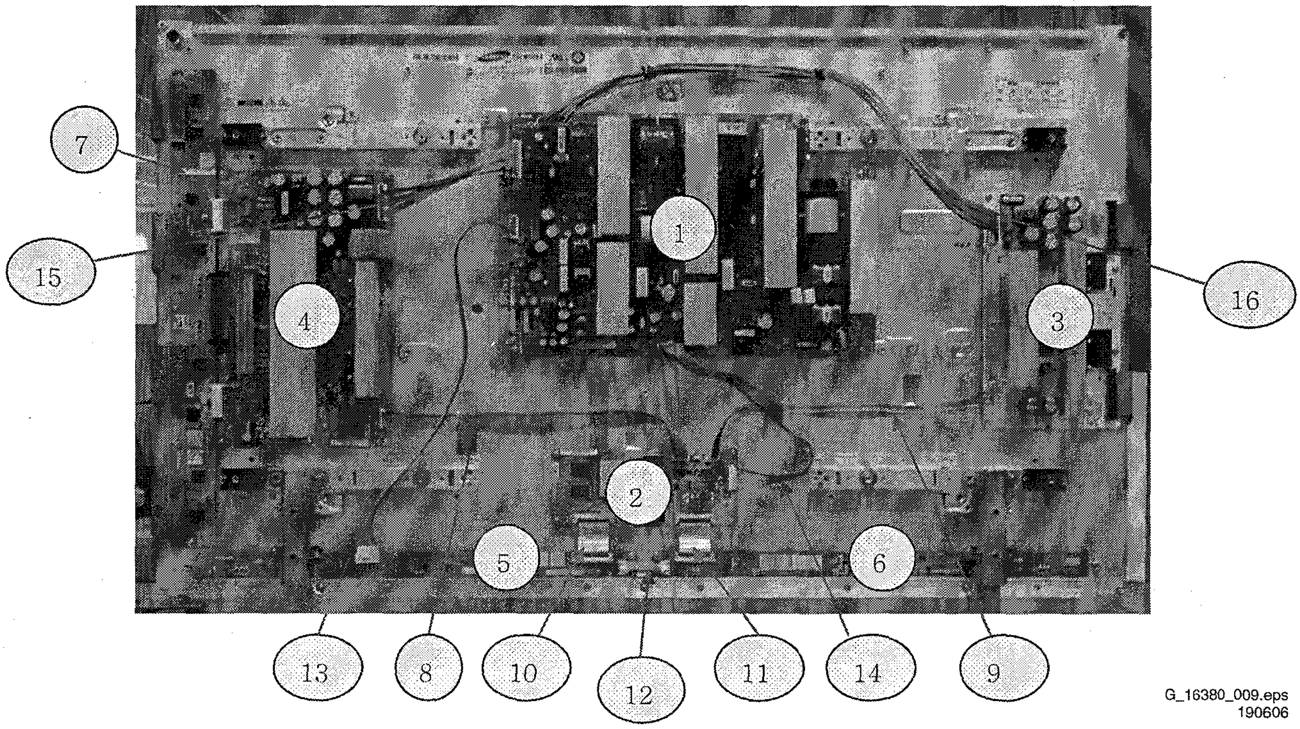

Figure 1-11 PWB location (42" SD v5)

Table 1-3 PWB overview (42" SD v5)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWB Logic Main
3	X-MAIN Driving Board	Assy PWB X Main
4	Y-MAIN Driving Board	Assy PWB Y Main
5	LOGIC E BUFFER Board	Assy PWB buffer
6	LOGIC F BUFFER Board	Assy PWB buffer
7	Y-BUFFER Board	Assy PWB buffer
8	LOGIC + Y-MAIN	Lead connector
9	LOGIC + X-MAIN	Lead connector
10	LOGIC + LOGIC BUF (E)	FFC cable-flat
11	LOGIC + LOGIC BUF (F)	FFC cable-flat
12	LOGIC BUF (E) + (F)	Lead connector
13	SMPS + LOGIC BUF (E)	Lead connector
14	SMPS + LOGIC MAIN	Lead connector
15	SMPS + Y-MAIN	Lead connector
16	SMPS + X-MAIN	Lead connector

1.3.2 42" HD w1

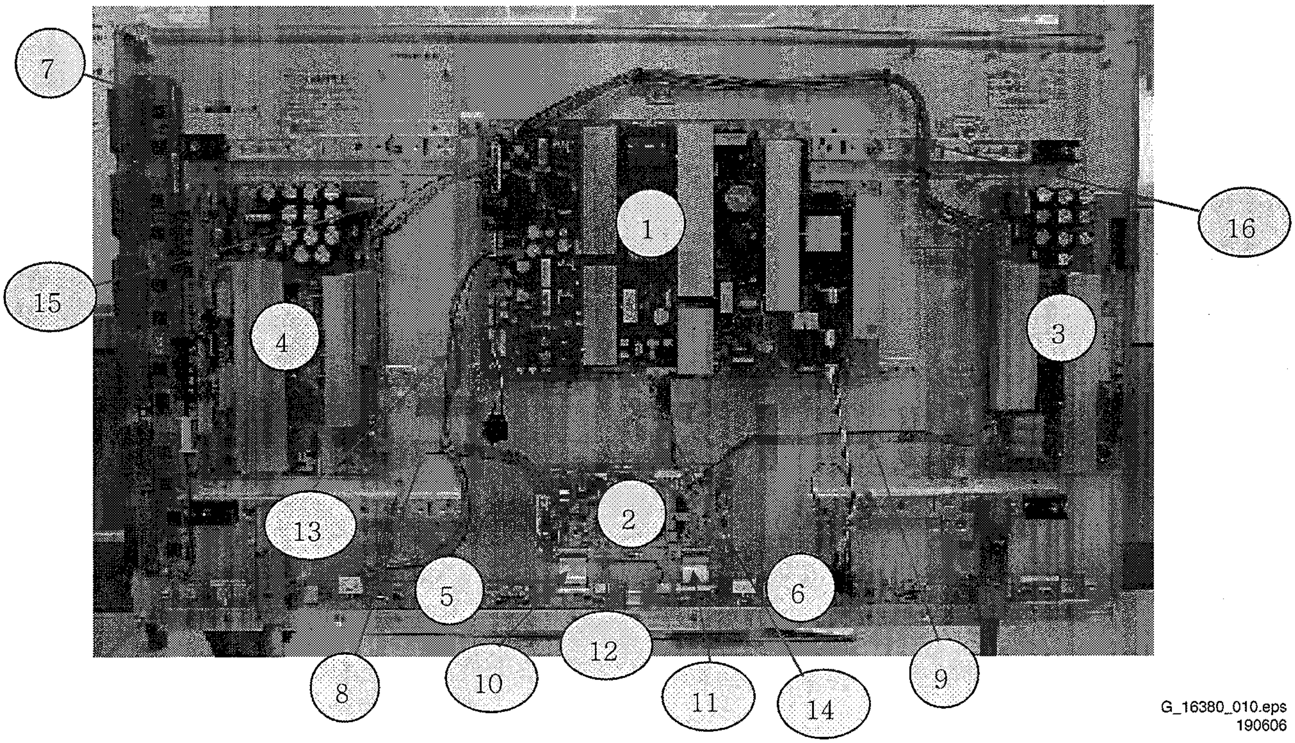

Figure 1-12 PWB location (42" HD w1)

Table 1-4 PWB overview (42" HD w1)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWB LOGIC Main
3	X-MAIN Driving Board	Assy PWB X Main
4	Y-MAIN Driving Board	Assy PWB Y Main
5	LOGIC E BUFFER Board	Assy PWB Buffer
6	LOGIC F BUFFER Board	Assy PWB Buffer
7	Y-BUFFER Board	Assy PWB Buffer
8	LOGIC + Y-MAIN	Lead connector
9	LOGIC + X-MAIN	Lead connector
10	LOGIC + LOGIC BUF(E)	FFC Cable-flat
11	LOGIC + LOGIC BUF(F)	FFC Cable-flat
12	LOGIC BUF(E) + LOG. BUF(F)	Lead connector
13	SMPS + LOGIC BUF(E)	Lead connector
14	SMPS + LOGIC MAIN	Lead connector
15	SMPS + Y-MAIN	Lead connector
16	SMPS + X-MAIN	Lead connector

1.3.3 50" HD w1

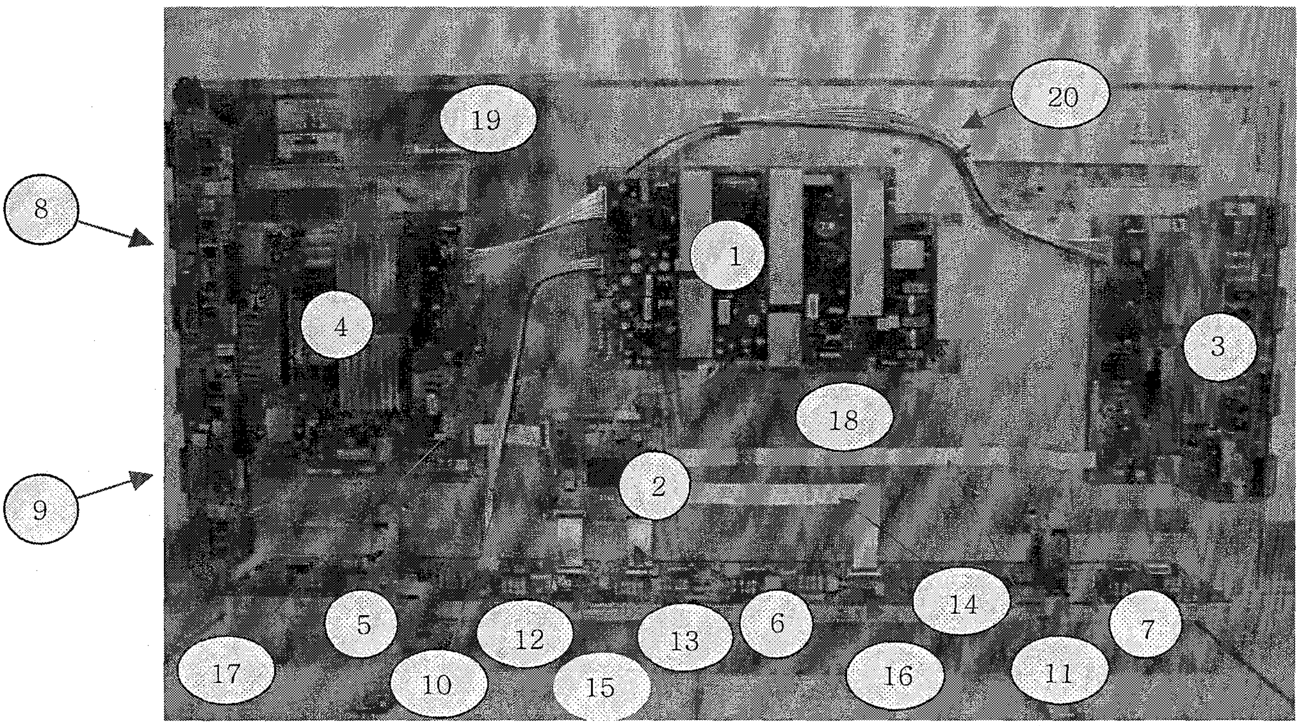

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Figure 1-13 PWB location (50" HD w5)

Table 1-5 PWB overview (50" HD w1)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWB LOGIC Main
3	X-MAIN Driving Board	Assy PWB X Main
4	Y-MAIN Driving Board	Assy PWB Y Main
5	LOGIC E BUFFER Board	Assy PWB Buffer E
6	LOGIC F BUFFER Board	Assy PWB Buffer F
7	LOGIC G BUFFER Board	Assy PWB Buffer G
8	Y-BUFFER (Upper) Board	Assy PWB Buffer
9	Y-BUFFER (Lower) Board	Assy PWB Buffer
10	LOGIC + Y-MAIN	FFC Cable-flat
11	LOGIC + X-MAIN	FFC Cable-flat
12	LOGIC + LOGIC BUF (E)	FFC Cable-flat
13	LOGIC + LOGIC BUF (F)	FFC Cable-flat
14	LOGIC + LOGIC BUF (G)	FFC Cable-flat
15	LOGIC BUF (E) + LOG. BUF (F)	Lead connector
16	LOGIC BUF (F) + LOG. BUF (G)	Lead connector
17	SMPS + LOGIC BUF (E)	Lead connector
18	SMPS + LOGIC MAIN	Lead connector
19	SMPS + Y-MAIN	Lead connector
20	SMPS + X-MAIN	Lead connector

1.3.4 63” HD v4

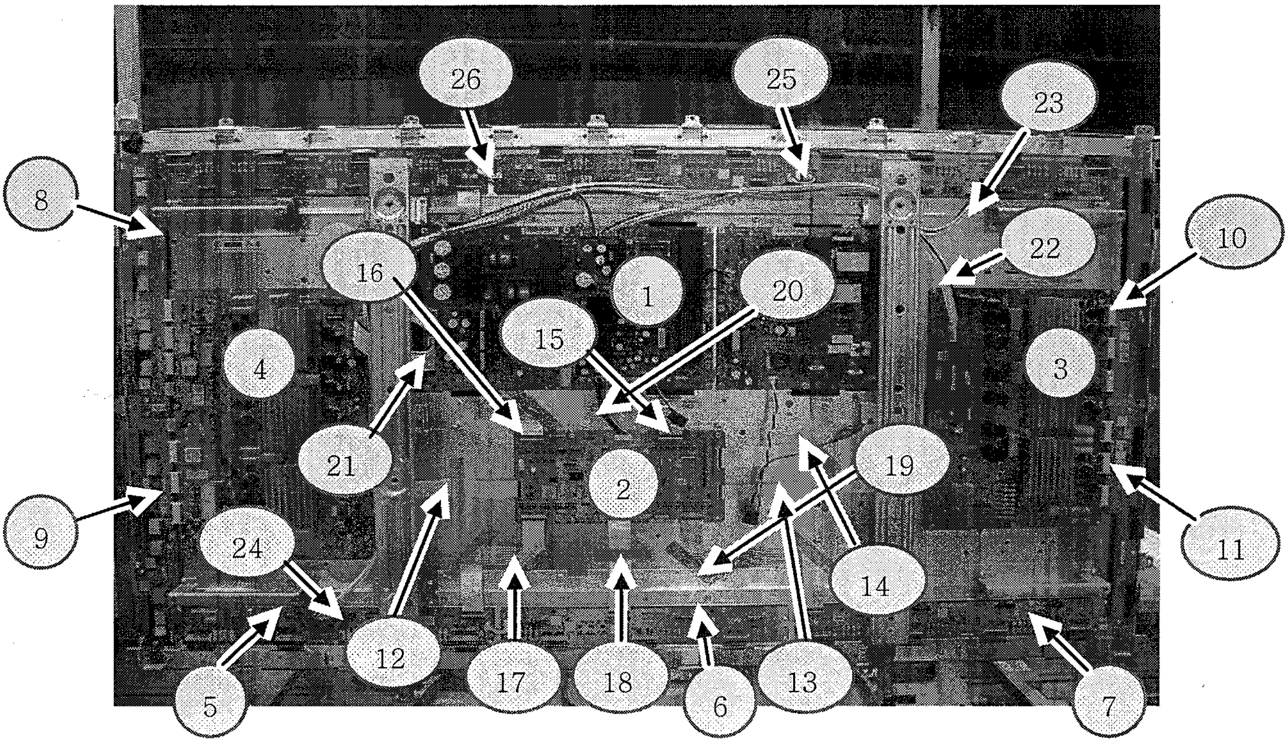

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Figure 1-14 PWB location (63” HD v4)

Table 1-6 PWB overview (50” HD w1)

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	Assy PWB LOGIC Main
3	X-MAIN Driving Board	Assy PWB X Main
4	Y-MAIN Driving Board	Assy PWB Y Main
5	LOGIC E BUFFER Board	Assy PWB Buffer E
6	LOGIC F BUFFER Board	Assy PWB Buffer F
7	LOGIC G BUFFER Board	Assy PWB Buffer G
8	Y-BUFFER (Upper) Board	Assy PWB Buffer
9	Y-BUFFER (Lower) Board	Assy PWB Buffer
10	X-BUFFER (Upper) Board	Assy PWB Buffer
11	X-BUFFER (Lower) Board	Assy PWB Buffer
12	LOGIC + Y-MAIN	FFC Cable-flat
13	LOGIC + X-MAIN	FFC Cable-flat
14	LOGIC + LOGIC BUF upper (E)	FFC Cable-flat
15	LOGIC + LOGIC BUF upper (F)	FFC Cable-flat
16	LOGIC + LOGIC BUF upper (G)	FFC Cable-flat
17	LOGIC + LOGIC BUF lower (E)	FFC Cable-flat
18	LOGIC + LOGIC BUF lower (F)	FFC Cable-flat
19	LOGIC + LOGIC BUF lower (G)	FFC Cable-flat
20	SMPS + LOGIC MAIN	Lead connector
21	SMPS + Y-MAIN	Lead connector
22	SMPS + X-MAIN	Lead connector
23	SMPS + LOGIC BUF upper (E)	Lead connector
24	SMPS + LOGIC BUF lower (E)	Lead connector
25	LOGIC BUF (E) + LOG. BUF (F)	Lead connector
26	LOGIC BUF (F) + LOG. BUF (G)	Lead connector

2. Safety Instructions, Warnings, and Notes

Index of this chapter:

2.1 Handling Precautions
2.2 Safety Precautions
2.3 Notes

Notes:

- Only authorised persons should perform servicing of this module.
- When using/handling this unit, pay special attention to the PDP Module: it should not be enforced into any other way then next rules, warnings, and/or cautions.
- **"Warning"** indicates a hazard that may lead to death or injury if the warning is ignored and the product is handled incorrectly.
- **"Caution"** indicates a hazard that can lead to injury or damage to property if the caution is ignored and the product is handled incorrectly.

2.1 Handling Precautions

- The PDP module use high voltage that is dangerous to humans. Before operating the PDP, always check for dust to prevent short circuits. Be careful touching the circuit device when power is "on".
- The PDP module is sensitive to dust and humidity. Therefore, assembling and disassembling must be done in no dust place.
- The PDP module has a lot of electric devices. The service engineer must wear equipment (for example, earth ring) to prevent electric shock and working clothes to prevent electrostatic.
- The PDP module use a fine pitch connector which is only working by exactly connecting with flat cable. The operator must pay attention to a complete connection when connector is reconnected after repairing.
- The capacitor's remaining voltage in the PDP module's circuit board temporarily remains after power is "off". Operator must wait for discharging of remaining voltage during at least 1 minute.

2.2 Safety Precautions

2.2.1 Safety Precautions

- Before replacing a board, discharge forcibly the remaining electricity from the board.
- When connecting FFC and TCPs to the module, recheck that they are perfectly connected.
- To prevent electrical shock, be careful not to touch leads during circuit operations.
- To prevent the Logic circuit from being damaged due to wrong working, do not connect/disconnect signal cables during circuit operations.
- Do thoroughly adjustment of a voltage label and voltage-insulation.
- Before reinstalling the chassis and the chassis assembly, be sure to use all protective stuff including a nonmetal controlling handle and the covering of partitioning type.
- Caution for design change: Do not install any additional devices to the module, and do not change the electrical circuit design.
- For example: Do not insert a subsidiary audio or video connector. If you insert It, it cause danger on safety. And, if you change the design or insert, manufacturer guarantee will be not effect.
- If any parts of wire is overheats of damaged, replace it with a new specified one immediately, and identify the cause of the problem and remove the possible dangerous factors.
- Examine carefully the cable status if it is twisted or damaged or displaced. Do not change the space between parts and circuit board. Check the cord of AC power preparing damage.
- Product Safety Mark: Some of electric or implement material have special characteristics invisible that was related on safety. In case of the parts are changed with new one, even though the Voltage and Watt is higher than before, the Safety and Protection function will be lost.
- The AC power always should be turned "off", before next repair.
- Check assembly condition of screw, parts and wire arrangement after repairing. Check whether the material around the parts get damaged.

2.2.2 ESD Precautions

There are parts, which are easily damaged by electrostatics (for example Integrated Circuits, FETs, etc.) Electrostatic damage rate of product will be reduced by the following technics:

- Before handling semiconductor parts/assembly, must remove positive electric by ground connection, or must wear the antistatic wrist-belt and ring (it must be operated after removing dust on it. It comes under precaution of electric shock).
- After removing the assembly, lay it with the tracks on a conductive surface to prevent charging.
- Do not use chemical stuff containing Freon. It generates positive electric that can damage ESD sensitive devices.
- You must use a soldering device for ground-tip when soldering or de-soldering these devices.
- You must use anti-static solder removal device. Most removal devices do not have antistatic which can charge a enough positive electric enough for damaging these devices.
- Before removing the protective material from the lead of a new device, bring the protective material into contact with the chassis or assembly.
- When handing an unpacked device for replacement, do not move around too much. Moving (legs on the carpet, for example) generates enough electrostatic to damage the device.
- Do not take a new device from the protective case until the it is ready to be installed. Most devices have a lead, which is easily short-circuited by conductive materials (such as conductive foam and aluminium)

2.3 Notes

A glass plate is positioned before the plasma display. This glass plate can be cleaned with a slightly humid cloth. If due to circumstances there is some dirt between the glass plate and the plasma display panel, it is recommended to do some maintenance by a qualified service employee only.

2.3.1 Safe PDP Handling

- The work procedures shown with the "Note" indication are important for ensuring the safety of the product and the servicing work. Be sure to follow these instructions.
- Before starting the work, secure a sufficient working space.
- At all times, other than when adjusting and checking the product, be sure to turn "off" the main POWER switch and disconnect the power cable from the power source of the display (jig or the display itself) during servicing.
- To prevent electric shock and breakage of PWBs, start the servicing work at least 30 seconds after the main power has been turned "off". Especially when installing and removing the Power Supply PWB and the SUS PWB in which high voltages are applied, start servicing at least 2 minutes after the main power has been turned "off".

- While the main power is "on", do not touch any parts or circuits other than the ones specified. The high voltage Power Supply block within the PDP module has a floating ground. If any connection other than the one specified is made between the measuring equipment and the high voltage power supply block, it can result in electric shock or activation of the leakage-detection circuit breaker.
- When installing the PDP module in, and removing it from the packing carton, be sure to have at least two persons perform the work while being careful to ensure that the flexible printed-circuit cable of the PDP module does not get caught by the packing carton.
- When the surface of the panel comes into contact with the cushioning materials, be sure to confirm that there is no foreign matter on top of the cushioning materials before the surface of the panel comes into contact with the cushioning materials. Failure to observe this precaution may result in, the surface of the panel being scratched by foreign matter.
- When handling the circuit PWB, be sure to remove static electricity from your body before handling the circuit PWB.
- Be sure to handle the circuit PWB by holding the large parts as the heat sink or transformer. Failure to observe this precaution may result in the occurrence of an abnormality in the soldered areas.
- Do not stack the circuit PWB. Failure to observe this precaution may result in problems resulting from scratches on the parts, the deformation of parts, and short-circuits due to residual electric charge.
- Routing of the wires and fixing them in position must be done in accordance with the original routing and fixing configuration when servicing is completed. All the wires are routed far away from the areas that become hot (such as the heat sink). These wires are fixed in position with the wire clamps so that the wires do not move, thereby ensuring that they are not damaged and their materials do not deteriorate over long periods of time. Therefore, route the cables and fix the cables to the original position and states using the wire clamps.
- Perform a safety check when servicing is completed. Verify that the peripherals of the serviced points have not undergone any deterioration during servicing. Also verify that the screws, parts and cables removed for servicing purposes have all been returned to their proper locations in accordance with the original

3. Directions For Use

Not applicable.

4. Mechanical Instructions

Index of this chapter:

4.1 Dis-assembling / Re-assembling
4.1.1 Flexible Printed Circuit of Y-Buffer (Upper and Lower)
4.1.2 Flat Cable Connector of X-main Board
4.1.3 FFC and TCP from Connector
4.1.4 Exchange of LBE and LBF board - 42" SD v5
4.1.5 Exchange of LBE and LBF board - 42" HD w1
4.1.6 Exchange of LBE, LBF and LBG board - 50" HD w1
4.1.7 Exchange of LB-E, LB-F and LB-G board - 63" HD v4
4.1.8 Exchange YB and YM board - 42" SD v5
4.1.9 Exchange YB and YM board - 42" HD w1
4.1.10 Exchange YBU, YBL and YM board - 50" HD w1
4.1.11 Exchange YBU, YBL and YM board - 63" HD v4

4.1 Dis-assembling / Re-assembling

4.1.1 Flexible Printed Circuit of Y-Buffer (Upper and Lower)

- Dis-assembly: Pull out the FPC from the connector by holding the lead of the FPC with both hands.
- Re-assembly: Push the lead of FPC with same force on both sides into the connector.

Note: Be careful not to damage the connector pin during connecting.

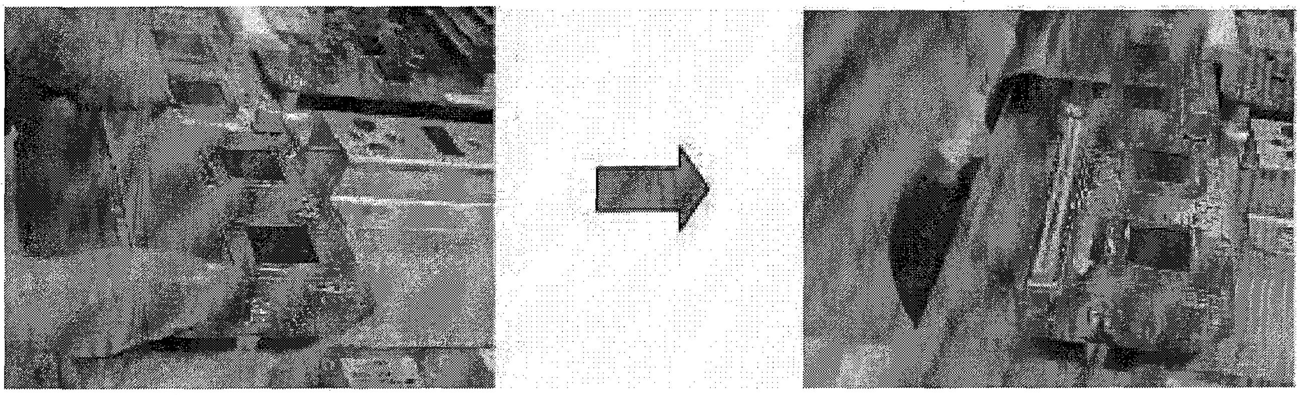

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Figure 4-1 Dis-assembly FPC of Y-buffer

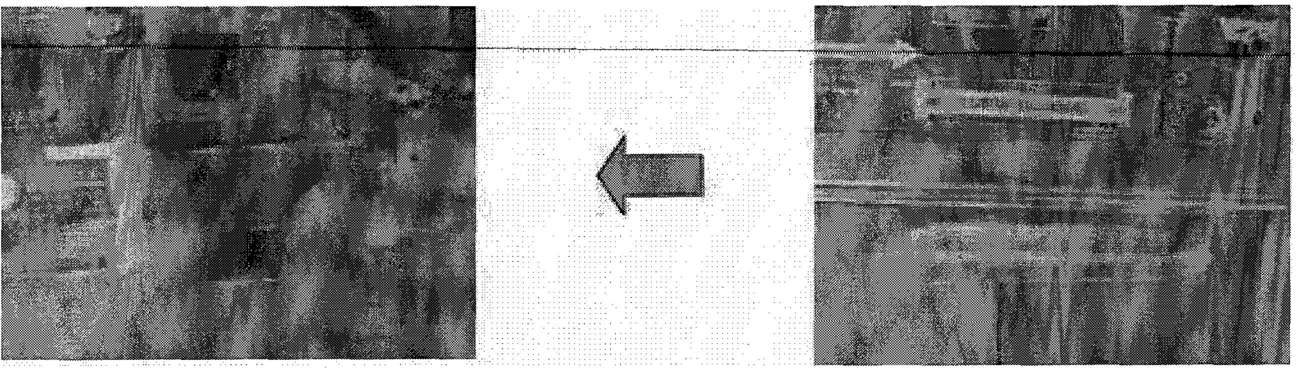

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Figure 4-2 Re-assembly FPC of Y-buffer

4.1.2 Flat Cable Connector of X-main Board

- Dis-assembly:
  1. Pull out the clamp of connector.
  2. Pull Flat cable out press down lightly.
  3. Turn the Flat Cable reversely.
- Re-assembly: Put the Flat Cable into the connector press down lightly until you hear a “Click“.

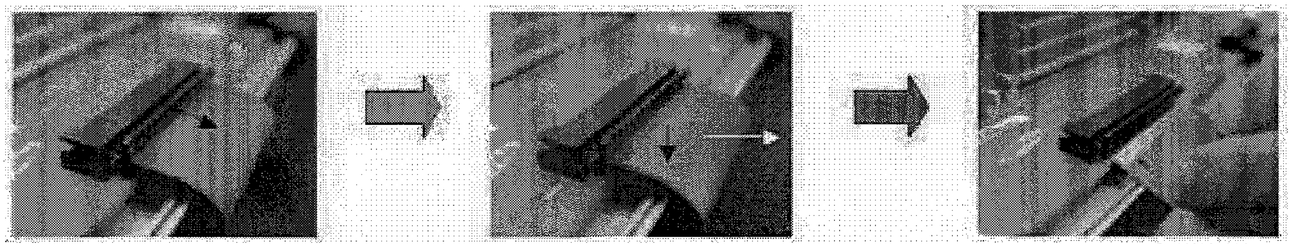
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Figure 4-3 Dis-assembly FCC of X-main board

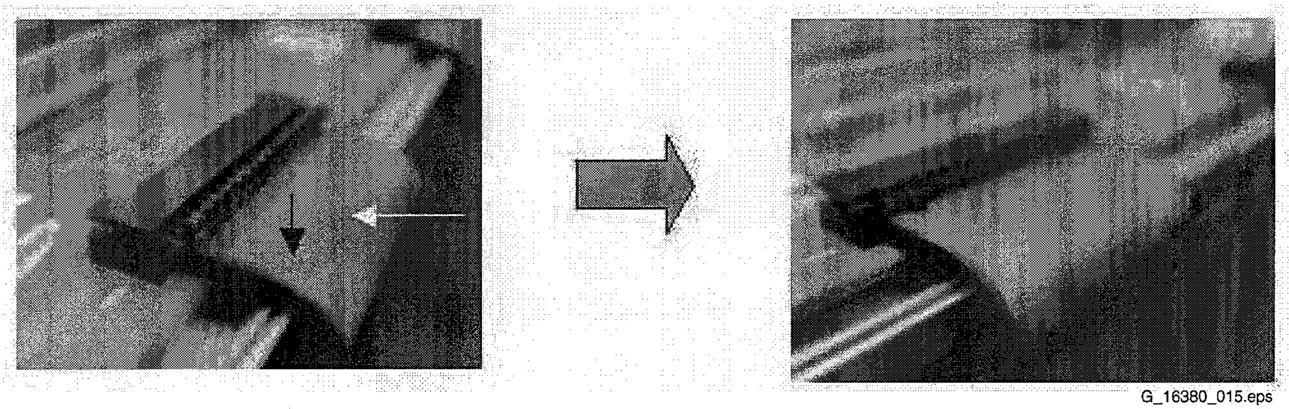
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Figure 4-4 Re-assembly FCC of X-main board

4.1.3 FFC and TCP from Connector

- Dis-assembling of TCP:
  1. Open the clamp carefully.
  2. Pull the TCP out from its connector.
- Re-assembling of TCP:
  1. Put the TCP into the connector carefully
  2. Close the clamp completely, until you hear a "Click".

Notes:

- Checking whether the foreign material is on the connector inside before assembling of TCP.
- Be careful, do not damage the board by ESD during handling of TCP.

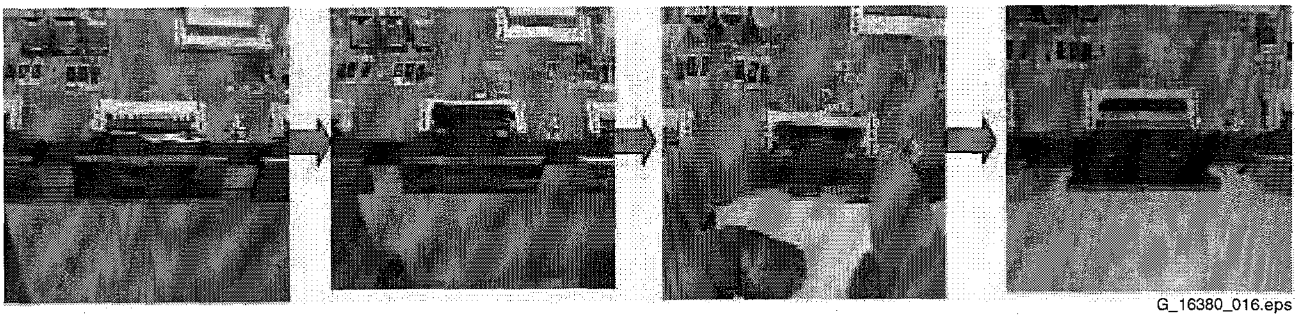

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Figure 4-5 Dis-assembly of TCP

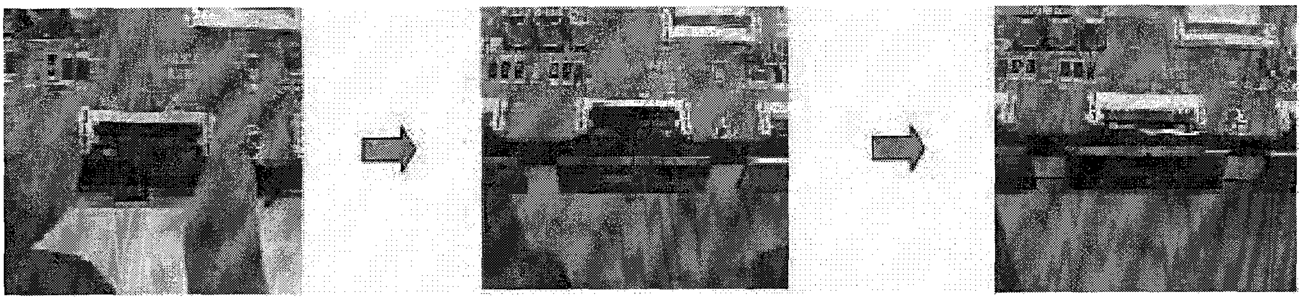

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Figure 4-6 Re-assembly of TCP

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Figure 4-7 Mis-assembly of TCP

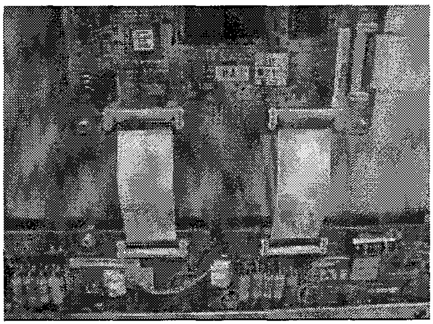

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Figure 4-8 Dis- and re-assembly of FFC

4.1.4 Exchange of LBE and LBF board - 42" SD v5

1. Remove the screws in order of 1-3-2 from the heatsink and remove the heatsink ("Photos 1 & 3")
2. Remove the TPC, FFC, and the power cable from the connectors.
3. Remove all the screws from the defective board ("Photo 2").
4. Remove the defective board.
5. Place the new board and screw it tight.
6. Clean the connectors.
7. Re-connect the TCP, FFC, and the power cable to the connectors.
8. Re-assemble the TCP heat sink. Use the screw mounting order 2-3-1.

Caution: If you screw too tight, it is possible to damage the Driver IC of the TCP.

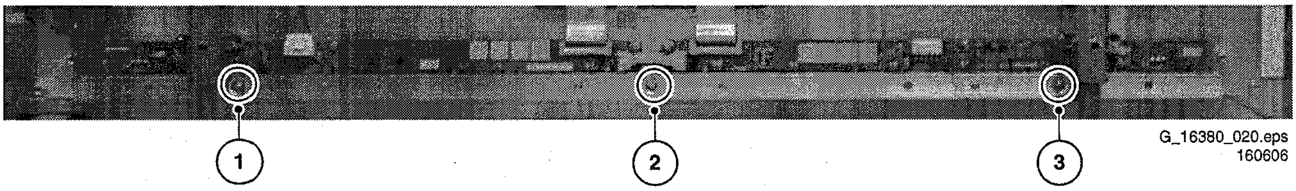

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Figure 4-9 Photo 1 - Heatsink 42" SD v5

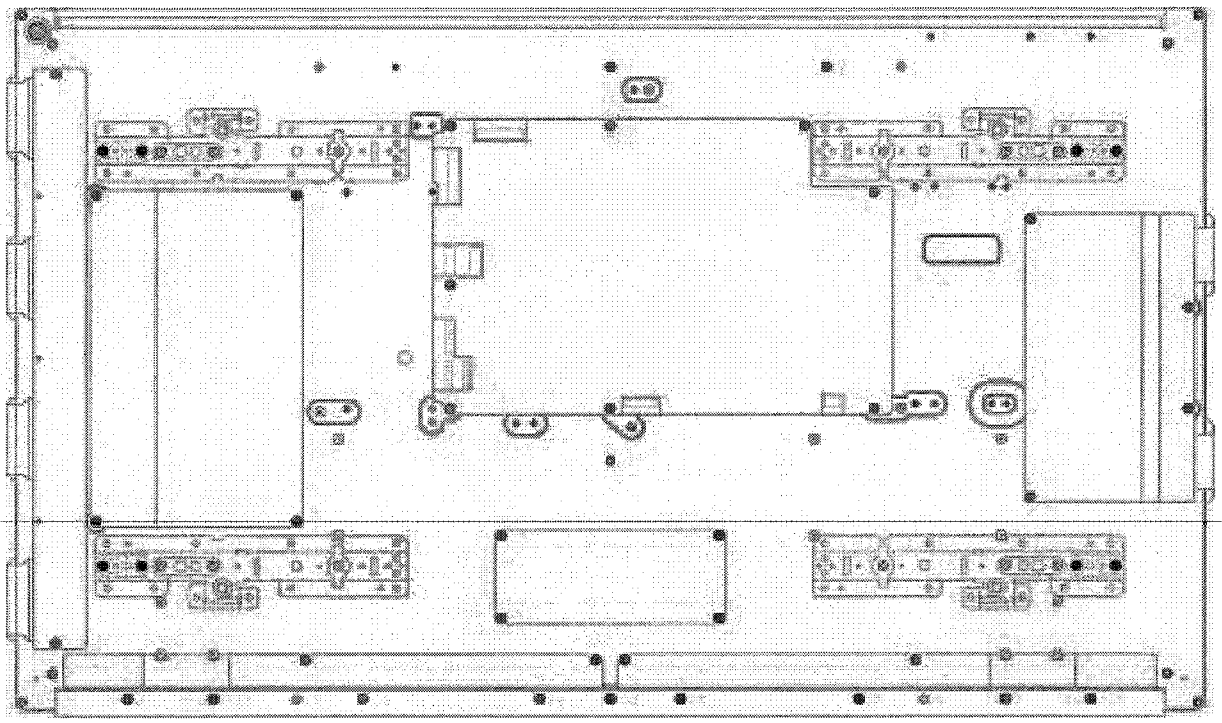

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Figure 4-10 Photo 2 - Exchange of LBE and LBF board 42" SD v5

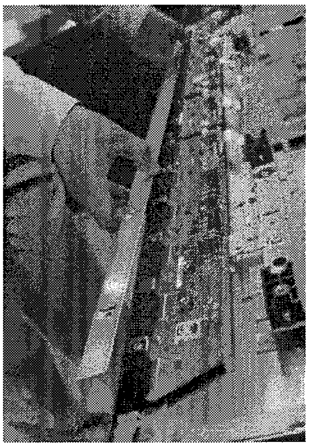

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Figure 4-11 Photo 3 - Heat sink removal

4.1.5 Exchange of LBE and LBF board - 42" HD w1

1. Remove the screws in order of 1-3-2 from the heatsink and remove the heatsink ("Photos 1 & 3").
2. Remove the TPC, FFC, and power cable from the connectors.
3. Remove all the screws from the defective board.
4. Remove the defective board.
5. Place the new board and then screw tightly.
6. Clean the connectors.
7. Re-connect the TCP, FFC, and power cable to the connectors.
8. Re-assemble the TCP heat sink. Use the screw mounting order 2-1-3.

Caution: *If you screw too tight, it is possible to damage the Driver IC of the TCP.*

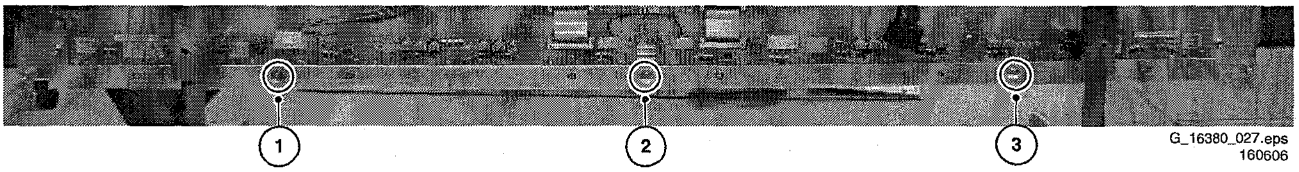

Figure 4-12 Photo 1 - Heatsink 42" HD w1

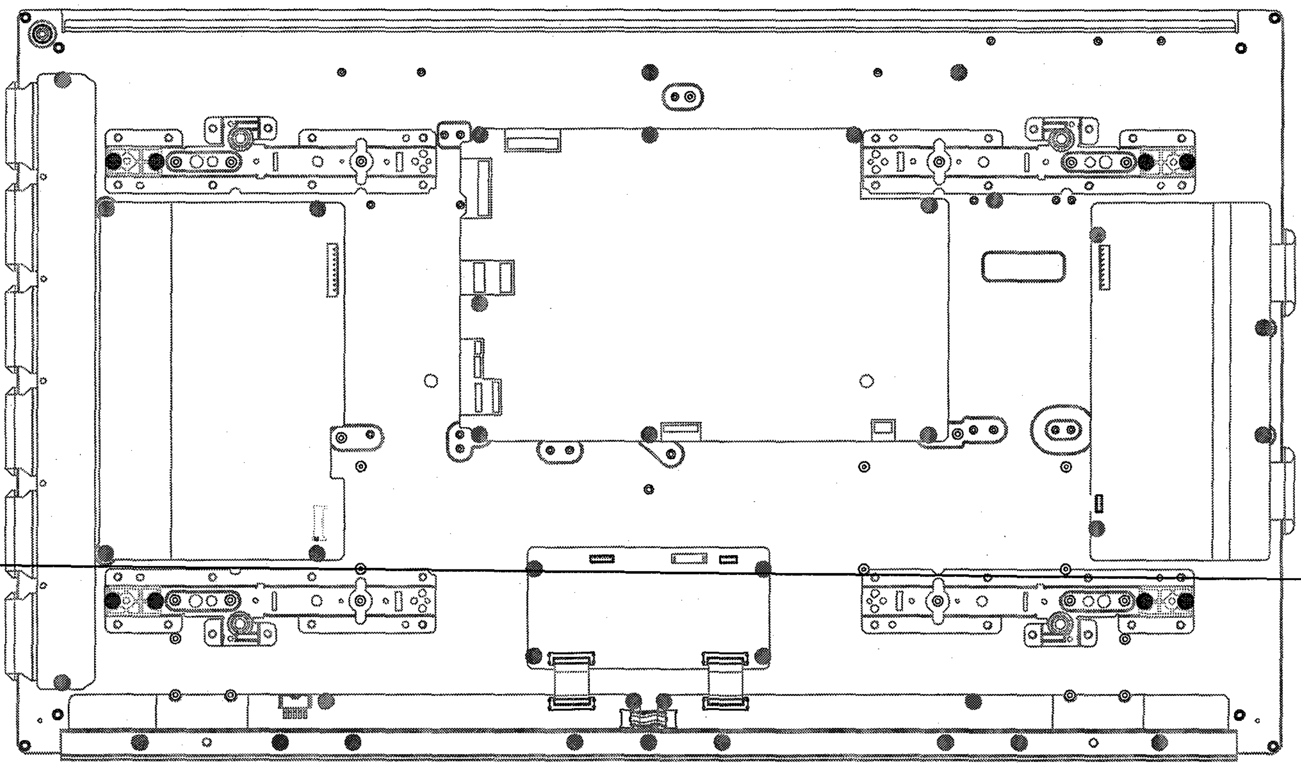

Figure 4-13 Photo 2 - Exchange of LBE, LBF board 42" HD w1

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Figure 4-14 Photo 3 - Heat sink removal

4.1.6 Exchange of LBE, LBF and LBG board - 50" HD w1

1. Remove the screws in order of 2-3-1-4 from the heatsink and remove the heatsink ("Photo 3").
2. Remove the TPC, FFC, and power cable from the connectors.
3. Remove all the screws from the defective board.
4. Remove the defective board.
5. Replace the new board and then screw tightly.
6. Clean the connectors.
7. Re-connect the TCP, FFC, and power cable to the connectors.
8. Re-assemble the TCP heat sink. Use the same screw mounting order as described above

Caution: If you screw too tight, it is possible to damage the Driver IC of the TCP.

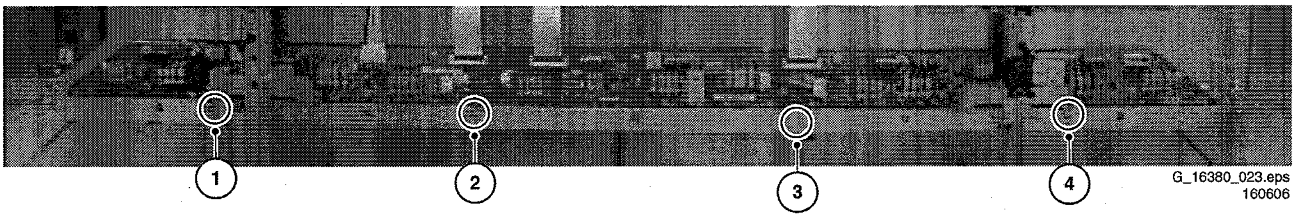

Figure 4-15 Photo 1 - Heatsink 50" HD w1

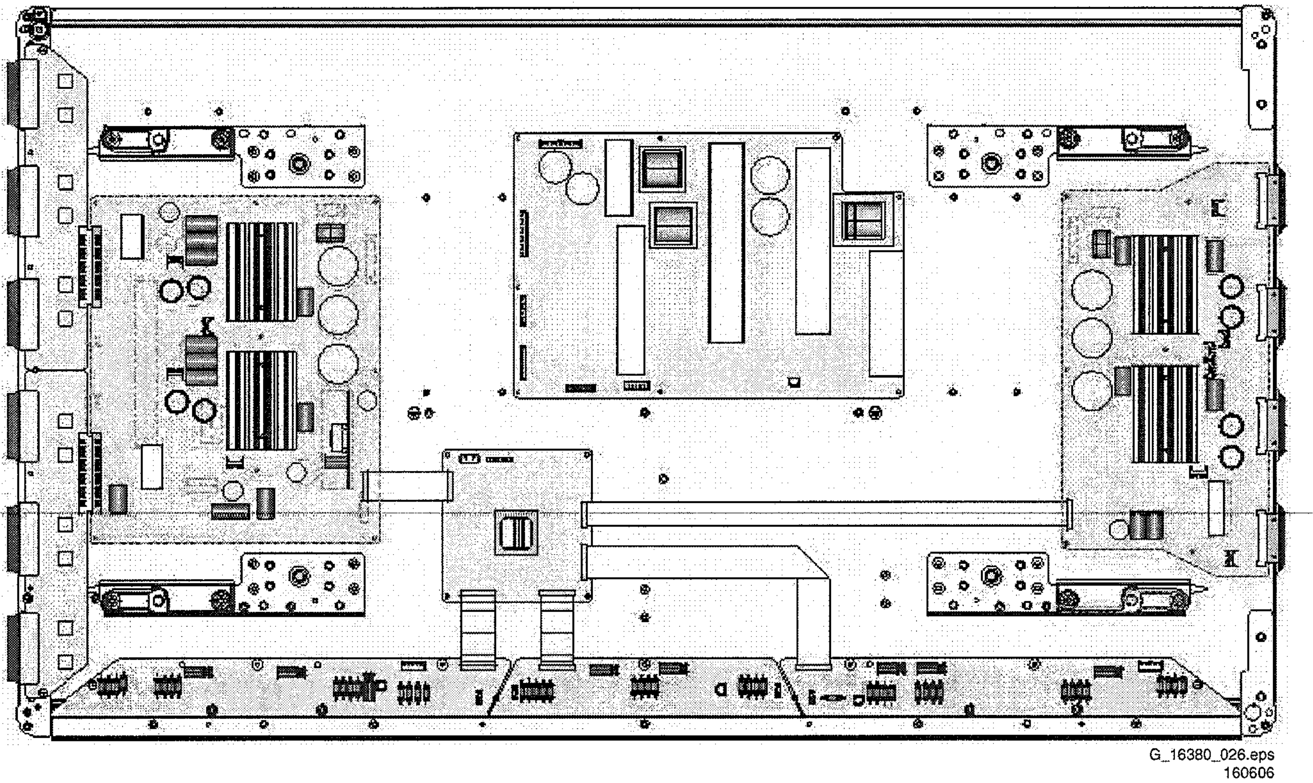

Figure 4-16 Photo 2 - Exchange of LBE, LBF, LBG board 50" HD w1

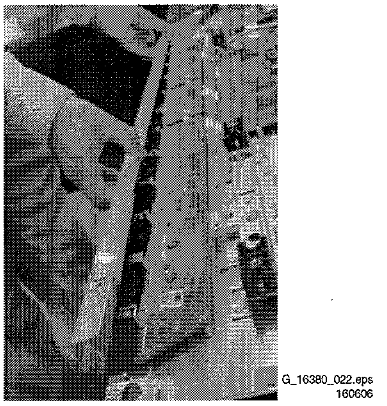

Figure 4-17 Photo 3 - Heat sink removal

4.1.7 Exchange of LB-E, LB-F and LB-G board - 63" HD v4

1. Refer to the Service Manual of the set to strip it so far, you have access to the Logic Buffer board that you need to replace.
2. For the lower LB-E, remove brackets [1] and [2]; for the lower LB-G, remove brackets [3] and [4]. For both LB-F's and the upper LB-E and LB-G you do not need to remove these brackets.
   Note: The following description is correct for the lower LBG; the replacement procedure of the other LB's is similar.
3. Remove the fixation screws [5] from the TPC heatsinks of the defective board.
4. Unplug the TPC, FFC, and power cable(s) from the connectors [6].
5. Remove the fixation screws from the defective board [7].
6. Remove the defective board.
7. Replace the new board and then screw tightly.
8. Clean the connectors.
9. Re-connect the TCP, FFC, and power cable to the connectors.
10. Re-assemble the TCP heat sinks. Slide the heatsink against strip [8] before you tighten it.

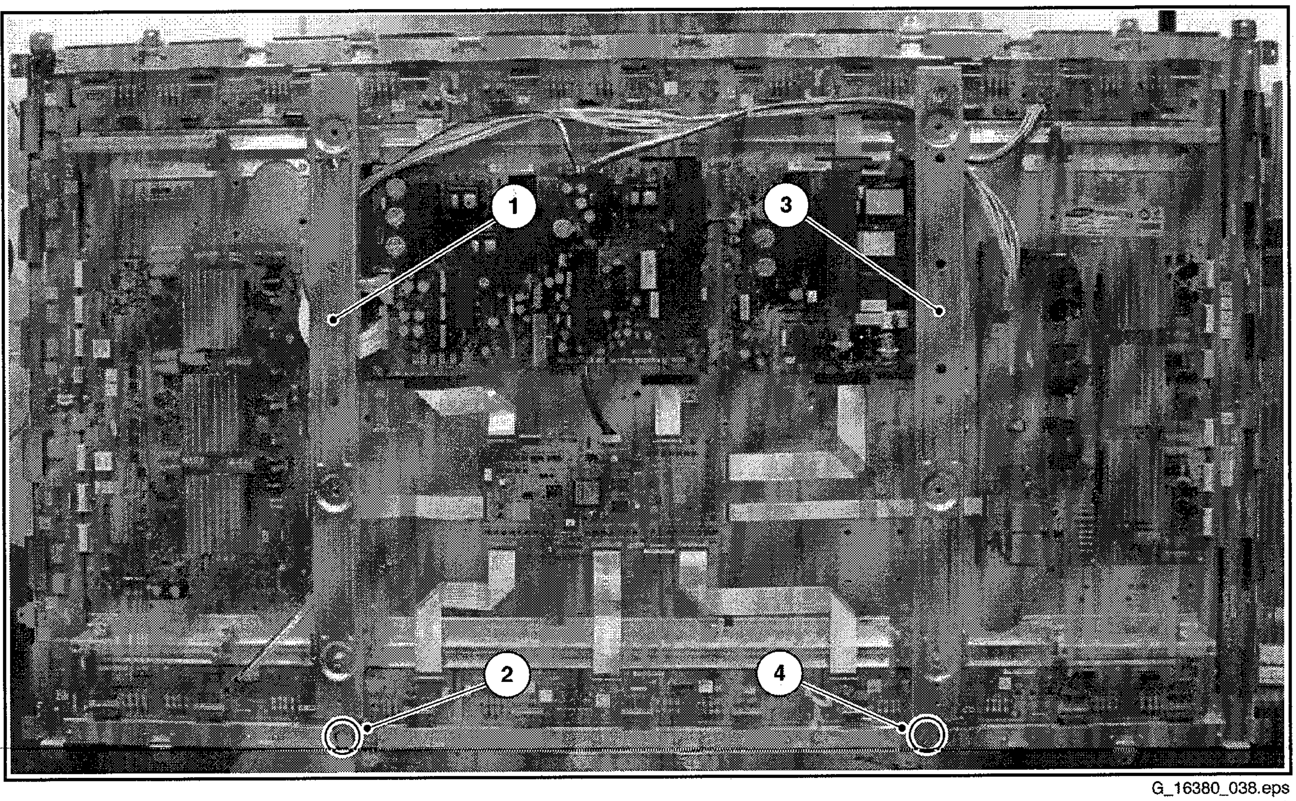

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Figure 4-18 Brackets 63" HD v4

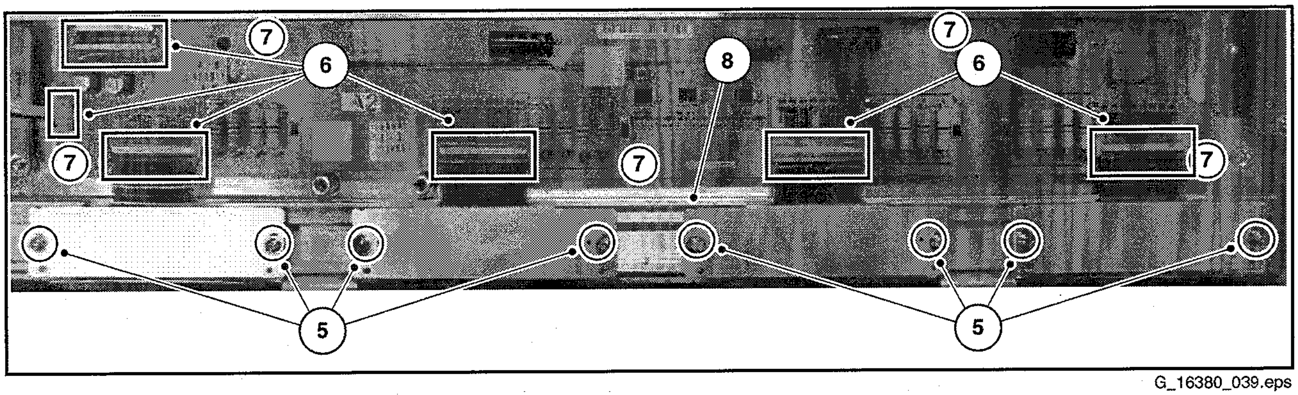

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Figure 4-19 Exchange of lower LB-G board 63" HD v4

4.1.8 Exchange YB and YM board - 42” SD v5

1. Unplug all of the FPC connectors of Y-Buffer. See “Photo 1”.
2. Unplug connectors CN5001 and CN5008 from Y-Main. See “Photo 2”.
3. Loosen all the screws of Y-Buffer and Y-Main. See “Photo 3”.
4. Remove the board from the chassis.
5. Unplug connectors CN5003, CN5004 and CN5005 between Y-Buffer and Y-Main.
6. Remove Y-Buffer from Y-main.
7. Replace the defective board.
8. Re-assemble Y-Buffer and Y-Main.
9. Plug in connectors CN5003, CN5004 and CN5005 between Y-Buffer and Y-Main. See “Photo 4”.
10. Arrange the boards on the chassis and tighten them.
11. Connect the FPC connectors. See “Photo 5”.
12. Supply the electric power to the module and then check the waveform of the board.
13. Turn “off” the power after the waveform is adjusted.

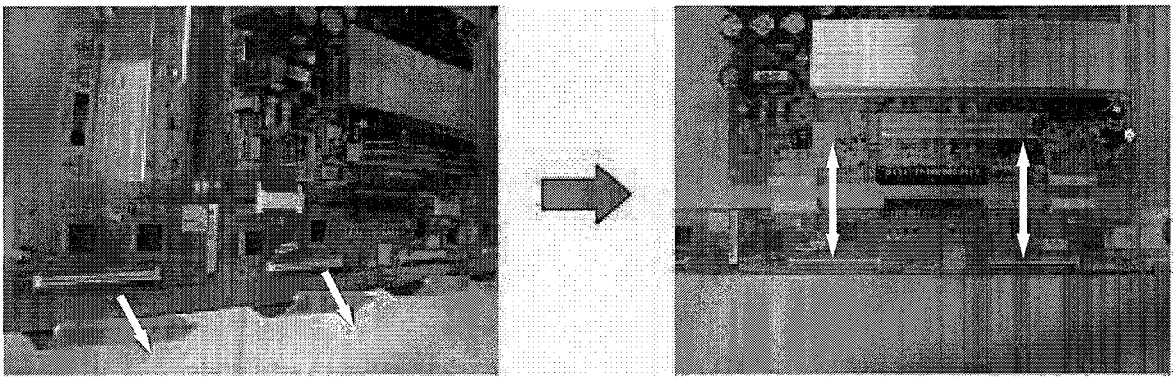
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Figure 4-20 Photo 1 and 2: Dis-assembly of YB and YM - 42” SD v5

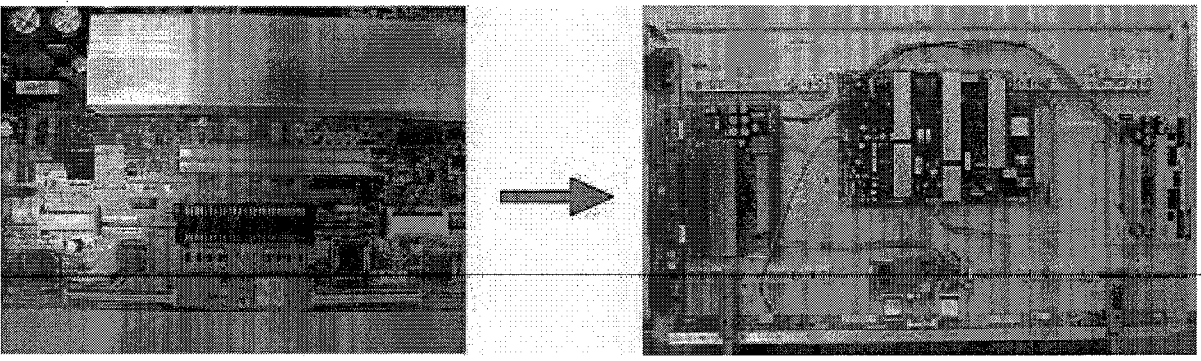
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Figure 4-21 Photo 3 and 4: Re-assembly of YB and YM - 42” SD v5

4.1.9 Exchange YB and YM board - 42” HD w1

1. Unplug all of the FPC connectors of Y-Buffer. See “Photo 1”.
2. Loosen all the screws of Y-Buffer and Y-Main. See “Photo 3”.
3. Remove the board from the chassis.
4. Unplug connectors CN5004, CN5011 and CN5012 between Y-Buffer and Y-Main.
5. Remove Y-Buffer from Y-main.
6. Replace the defective board.
7. Re-assemble Y-Buffer and Y-Main.
8. Plug in connectors CN5004, CN5011 and CN5012 between Y-Buffer and Y-Main. See “Photo 4”.
9. Arrange the boards on the chassis and tighten them.
10. Connect the FPC connectors.
11. Supply the electric power to the module and then check the waveform of the board.
12. Turn “off” the power after the waveform is adjusted.

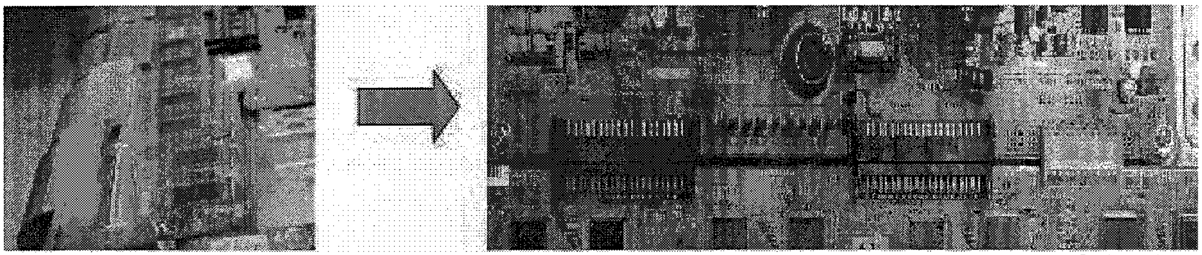
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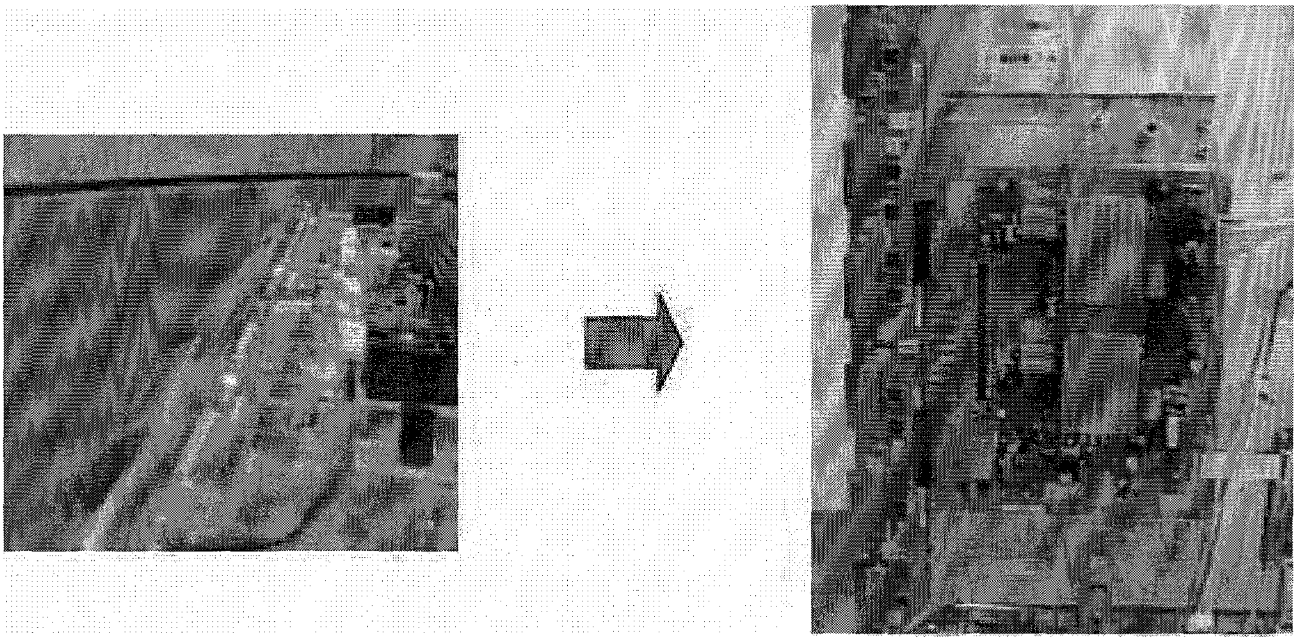
Figure 4-22 Photo 1 and 2: Dis-assembly of YBU, YBL, and YM - 42” HD w1

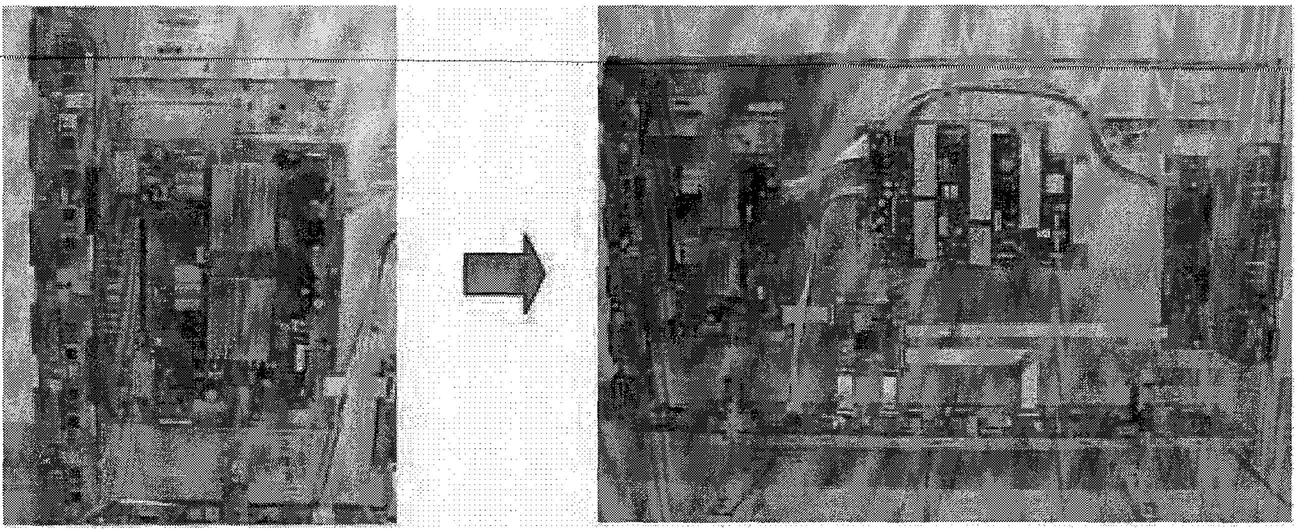
4.1.10 Exchange YBU, YBL and YM board - 50" HD w1

1. Unplug all of the FPC connectors of YBU (Y-Buffer upper) and YBL (Y-Buffer lower). See "Photo 1".
2. Unplug the connector CN5412 between YBU and YBL.
3. Loosen all the screws of YBU, YBL, and Y-Main.
4. Remove the board from the chassis.
5. Remove the YBL and YBU from Y-main.
6. Replace the defective board.
7. Re-assemble the YBU and YBL to the Y-Main.
8. Plug in connector CN5412 between YBU and YBL.
9. Arrange the board on the chassis and then screw to fix.
10. Connect the FPCs.
11. Supply the electric power to the module and then check the waveform of the board.
12. Turn "off" the power after the waveform is adjusted.



G_16380_033.eps
190606

Figure 4-23 Photo 1 and 2: Dis-assembly of YBU, YBL, and YM - 50" HD w1

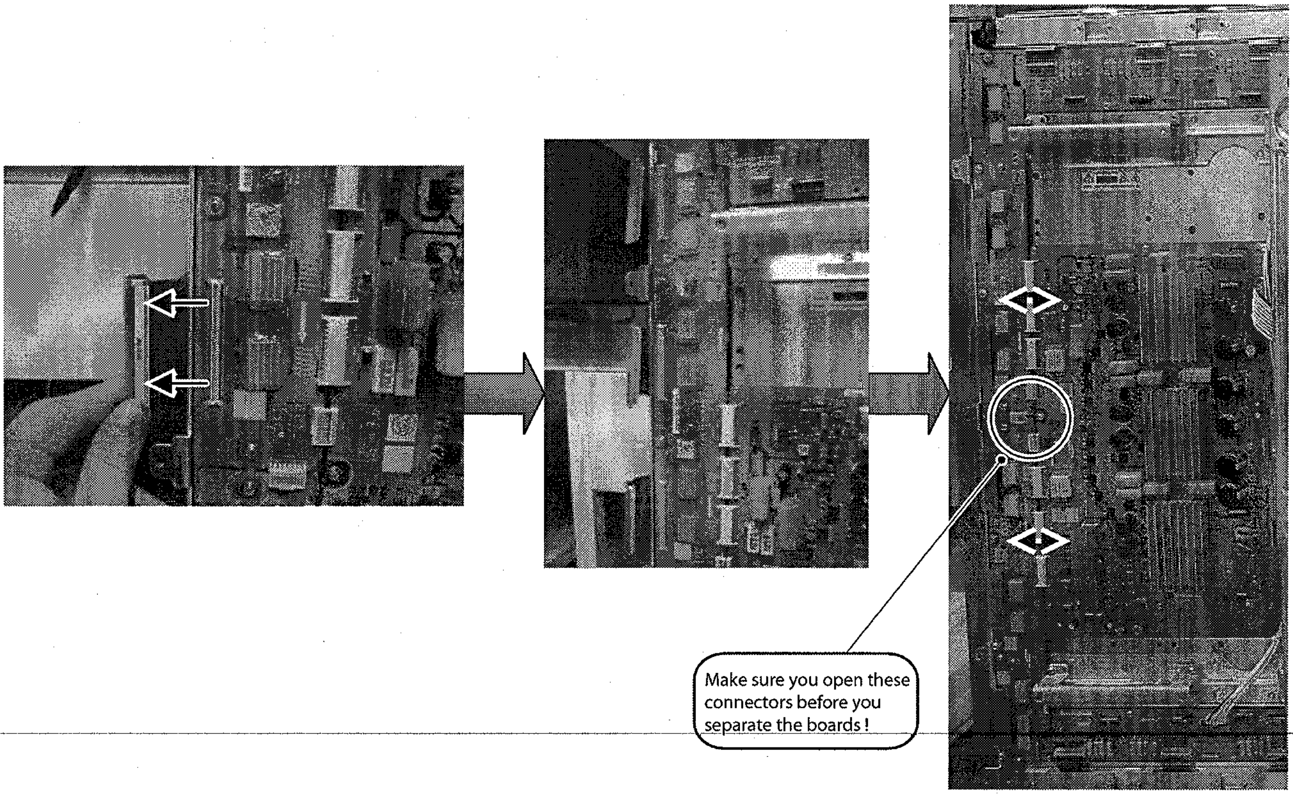


G_16380_034.eps
190606

Figure 4-24 Photo 3 and 4: Re-assembly of YBU, YBL, and YM - 50" HD w1

4.1.11 Exchange YBU, YBL and YM board - 63” HD v4

1. Unplug power connector CN5010 and signal connector CN5002 from Y-Main. See “Photo 1”.
2. Unplug all FPC connectors of YBU (Y-Buffer upper) and YBL (Y-Buffer lower). See “Photo 1”.
3. Open the connectors CN5001/CN5406 between YM and YBU, and CN5000/CN5506 between YM and YBL.
4. Loosen all the screws of YBU, YBL, and Y-Main.
5. Remove the boards from the chassis.
6. Open the connectors CN5410/CN5510 between YBU and YBL.
7. Separate the YBL and YBU from Y-main.
8. Replace the defective board.
9. Re-assemble the YBU and YBL to the Y-Main.
10. Plug in the connectors between YBU, YBL and YM.
11. Arrange the board on the chassis and then screw to fix.
12. Reconnect the FPCs.
13. Supply the electric power to the module and then check the waveform of the board.
14. Turn “OFF” the power after the waveform is adjusted.



Make sure you open these connectors before you separate the boards !

G_16380_042.eps
161006

Figure 4-25 Photo 1: Dis-assembly of YBU, YBL, and YM - 63” HD v4

5. Service Modes, Error Codes, and Fault Finding

Index of this chapter:

5.1 Repair Tools
5.1.1 ComPair
5.1.2 Other Service Tools
5.2 Fault Finding
5.2.1 Possible Scenarios
5.2.2 Faulty Power Supply
5.2.3 No Display
5.2.4 Abnormal display
5.2.5 Horizontal line or block open
5.2.6 Address open
5.2.7 Address short
5.2.8 Criteria for Panel Replacement, due to Defective Panel Cells
5.2.9 Overview
5.3 Defect Description Form

5.1 Repair Tools

5.1.1 ComPair

For the v5 and w1 models, it will be possible to generate test patterns with ComPair. The ComPair interface must be connected to the Logic Board with the special interconnection cable (see table below for the order code).

5.1.2 Other Service Tools

Table 5-1 Overview Service tools

Service Tools	Order Code
ComPair / SDI interconnection cable	3122 785 90800
Foam buffers (2 pcs.)	3122 785 90581

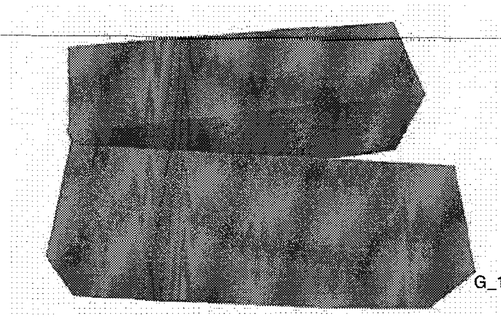


Figure 5-1 Foam buffers

5.2 Fault Finding

5.2.1 Possible Scenarios

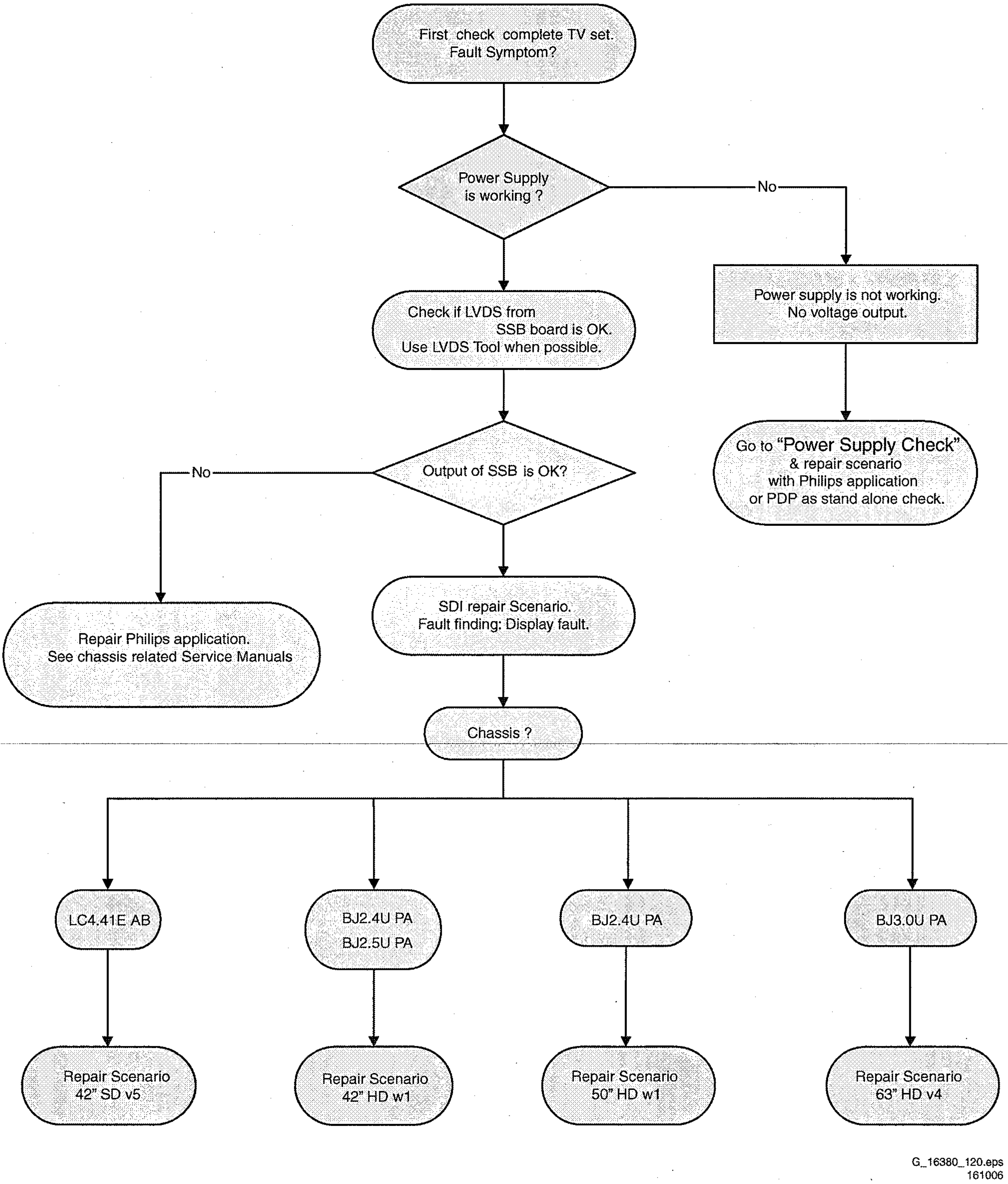

First check complete TV set.
Fault Symptom?
Power Supply is working ?
No
Power supply is not working.
No voltage output.
Go to "Power Supply Check" & repair scenario with Philips application or PDP as stand alone check.
Check if LVDS from SSB board is OK.
Use LVDS Tool when possible.
Output of SSB is OK?
No
Repair Philips application.
See chassis related Service Manuals
SDI repair Scenario.
Fault finding: Display fault.
Chassis ?
LC4.41E AB
BJ2.4U PA
BJ2.5U PA
BJ2.4U PA
BJ3.0U PA
Repair Scenario 42" SD v5
Repair Scenario 42" HD w1
Repair Scenario 50" HD w1
Repair Scenario 63" HD v4
G_16380_120.eps
161006

Figure 5-2 Which repair scenario?

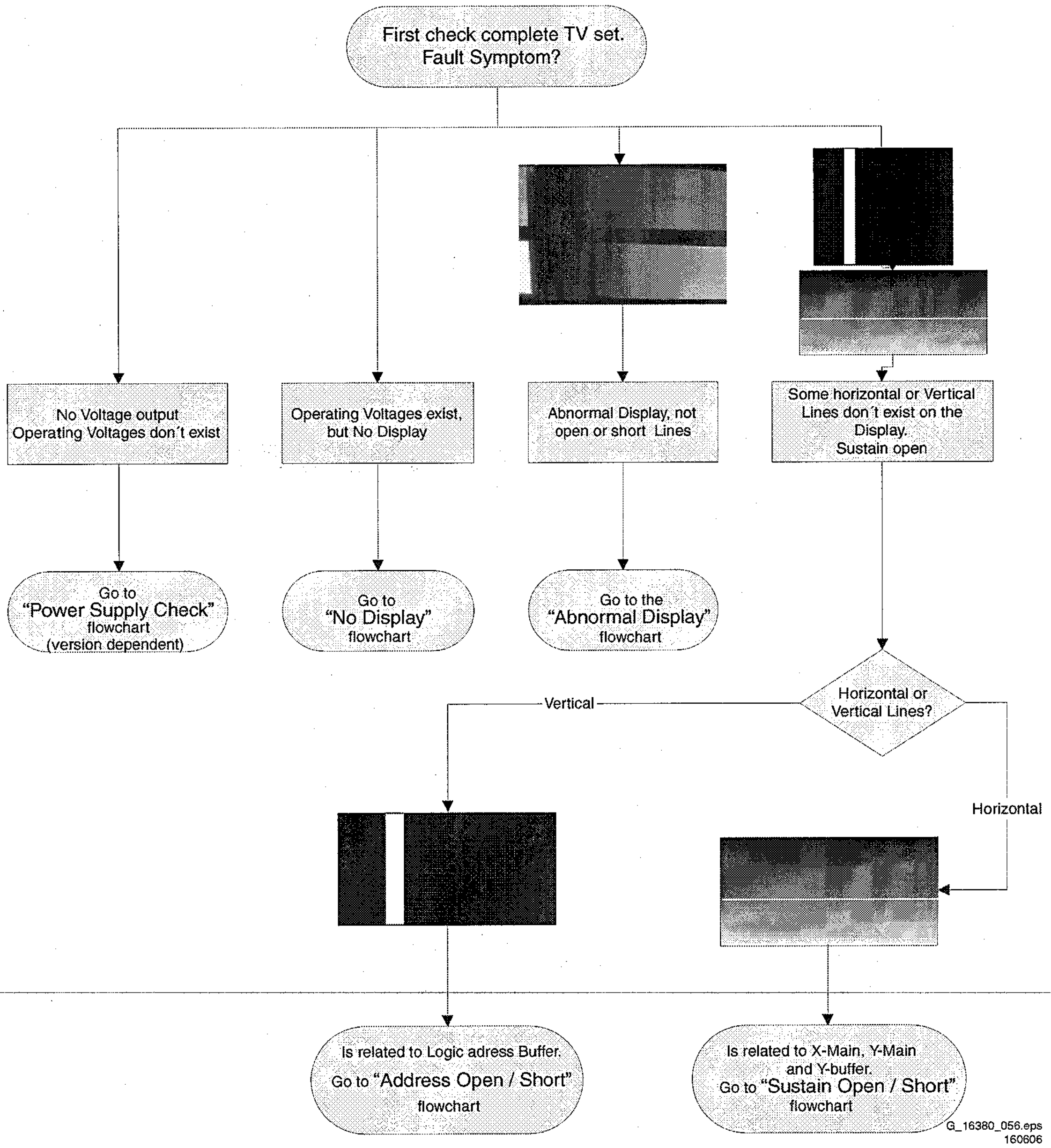

First check complete TV set.
Fault Symptom?
No Voltage output
Operating Voltages don´t exist
Operating Voltages exist, but No Display
Abnormal Display, not open or short Lines
Some horizontal or Vertical Lines don´t exist on the Display.
Sustain open
Go to "Power Supply Check" flowchart (version dependent)
Go to "No Display" flowchart
Go to the "Abnormal Display" flowchart
Horizontal or Vertical Lines?
Vertical
Horizontal
Is related to Logic adress Buffer.
Go to "Address Open / Short" flowchart
Is related to X-Main, Y-Main and Y-buffer.
Go to "Sustain Open / Short" flowchart
G_16380_056.eps
160606

Figure 5-3 Fault symptom overview (complete TV set)

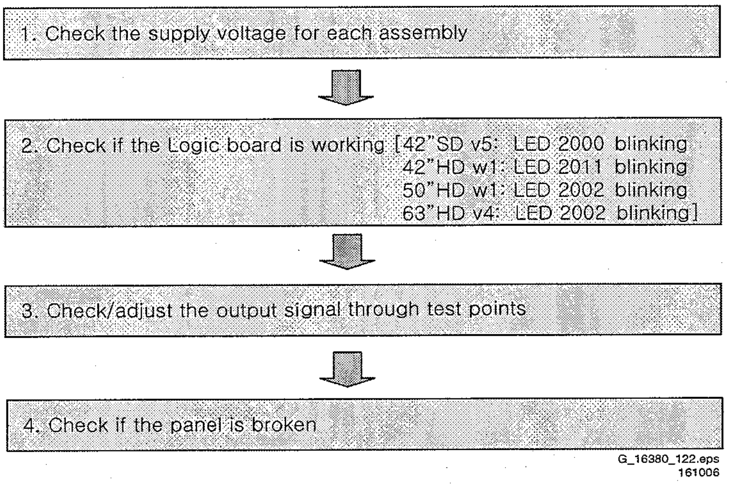

1. Check the supply voltage for each assembly
2. Check if the Logic board is working [42"SD v5: LED 2000 blinking
42"HD w1: LED 2011 blinking
50"HD w1: LED 2002 blinking
63"HD v4: LED 2002 blinking]
3. Check/adjust the output signal through test points
4. Check if the panel is broken
G_16380_122.eps
161006

Figure 5-4 Repair scenario stand alone panels

5.2.2 Faulty Power Supply

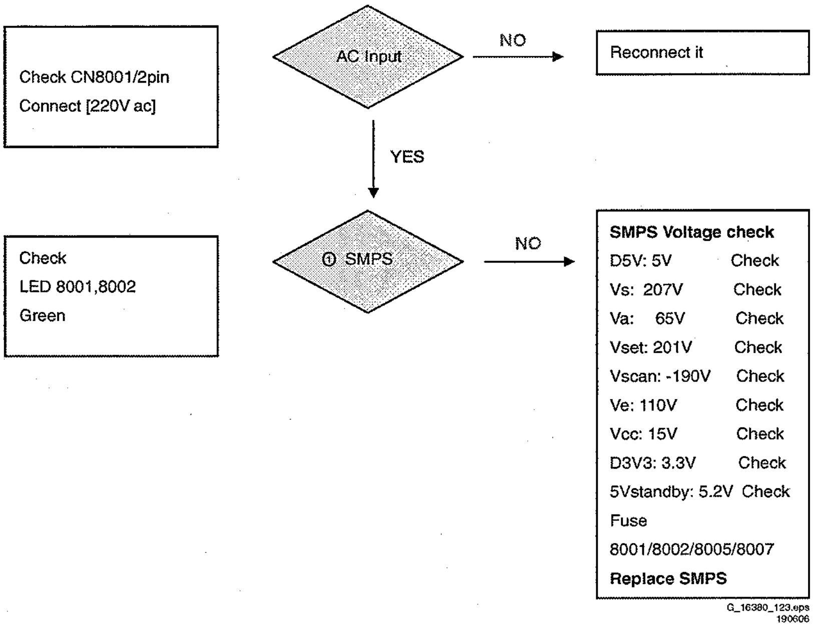

Check CN8001/2pin
Connect [220V ac]
AC Input
NO
Reconnect it
YES
Check
LED 8001,8002
Green
① SMPS
NO
SMPS Voltage check
D5V: 5V Check
Vs: 207V Check
Va: 65V Check
Vset: 201V Check
Vscan: -190V Check
Ve: 110V Check
Vcc: 15V Check
D3V3: 3.3V Check
5Vstandby: 5.2V Check
Fuse
8001/8002/8005/8007
Replace SMPS
G_16380_123.eps
190606

Figure 5-5 Power Supply Check for 42” SD v5 models 1/2

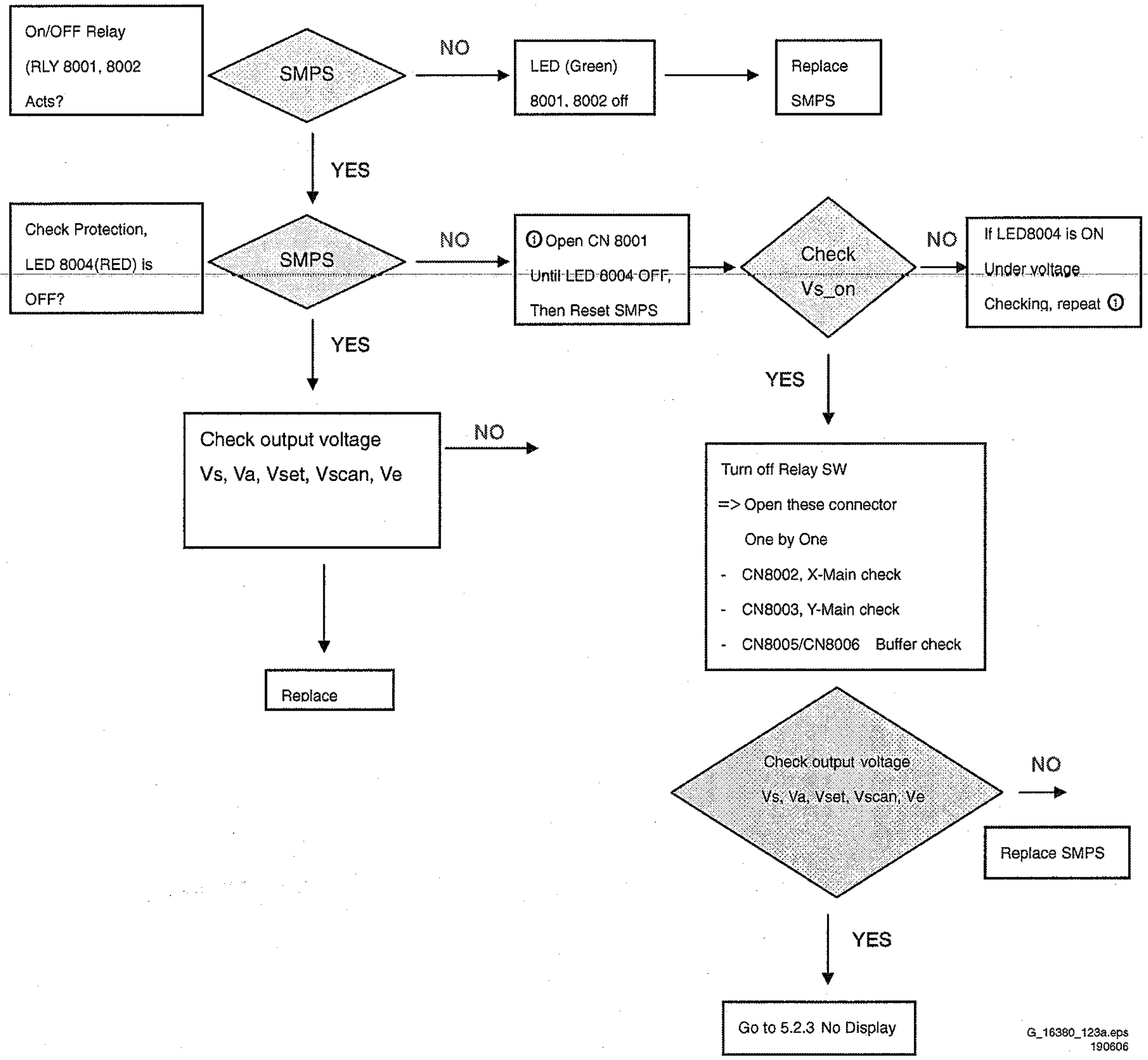

On/OFF Relay
(RLY 8001, 8002
Acts?
SMPS
NO
LED (Green)
8001, 8002 off
Replace
SMPS
YES
Check Protection,
LED 8004(RED) is
OFF?
SMPS
NO
① Open CN 8001
Until LED 8004 OFF,
Then Reset SMPS
Check
Vs_on
NO
If LED8004 is ON
Under voltage
Checking, repeat ①
YES
Check output voltage
Vs, Va, Vset, Vscan, Ve
NO
YES
Replace
Turn off Relay SW
=> Open these connector
One by One
- CN8002, X-Main check
- CN8003, Y-Main check
- CN8005/CN8006 Buffer check
Check output voltage
Vs, Va, Vset, Vscan, Ve
NO
Replace SMPS
YES
Go to 5.2.3 No Display
G_16380_123a.eps
190606

Figure 5-6 Power Supply Check for 42” SD v5 models 2/2

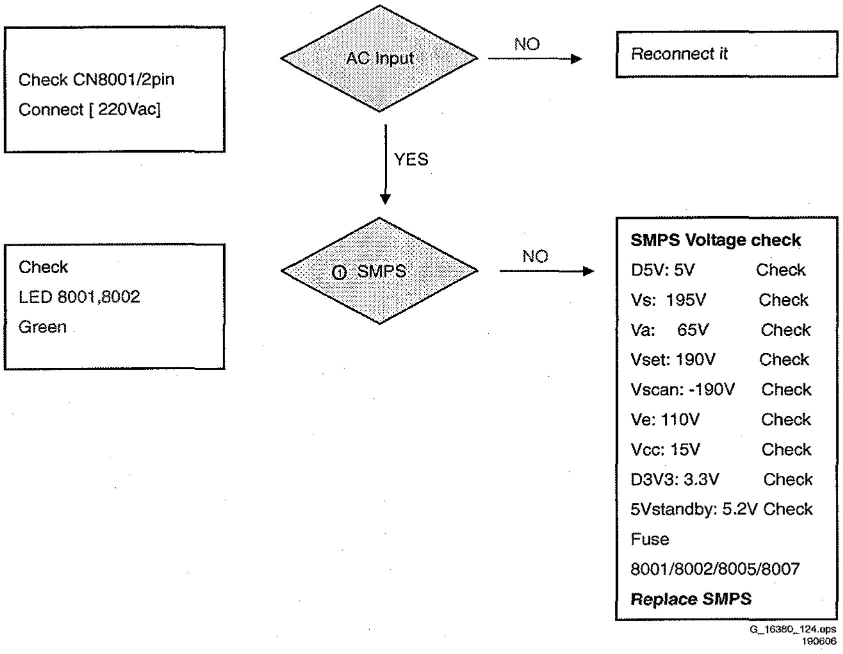

Check CN8001/2pin
Connect [220Vac]
AC Input
NO
Reconnect it
YES
Check
LED 8001,8002
Green
① SMPS
NO
SMPS Voltage check
D5V: 5V Check
Vs: 195V Check
Va: 65V Check
Vset: 190V Check
Vscan: -190V Check
Ve: 110V Check
Vcc: 15V Check
D3V3: 3.3V Check
5Vstandby: 5.2V Check
Fuse
8001/8002/8005/8007
Replace SMPS
G_16380_124.eps
190606

Figure 5-7 Power Supply Check for 42” HD w1 models 1/2

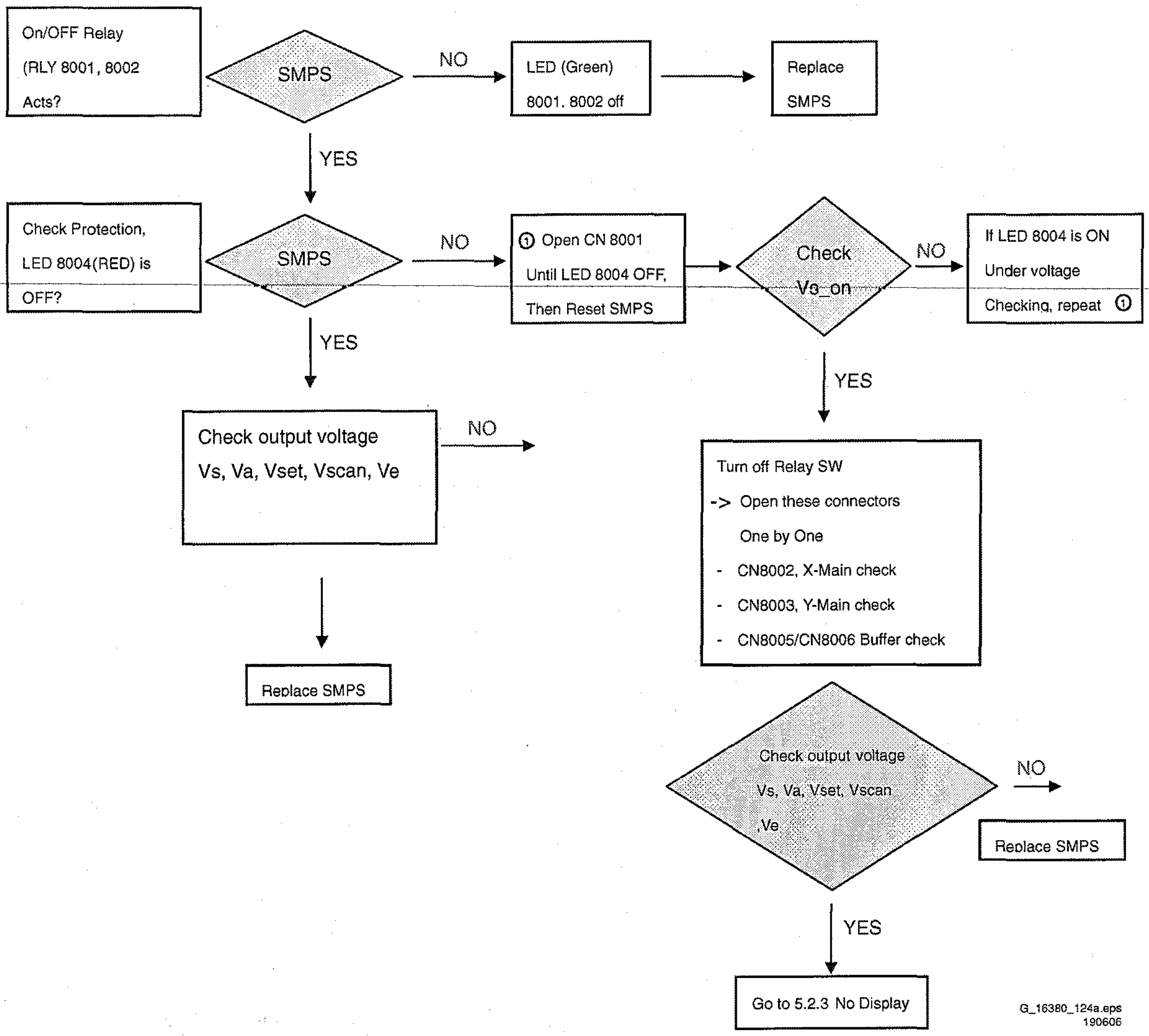

On/OFF Relay
(RLY 8001, 8002
Acts?
SMPS
NO
LED (Green)
8001. 8002 off
Replace
SMPS
YES
Check Protection,
LED 8004(RED) is
OFF?
SMPS
NO
① Open CN 8001
Until LED 8004 OFF,
Then Reset SMPS
Check
Vs_on
NO
If LED 8004 is ON
Under voltage
Checking, repeat ①
YES
YES
Check output voltage
Vs, Va, Vset, Vscan, Ve
NO
Replace SMPS
Turn off Relay SW
-> Open these connectors
One by One
- CN8002, X-Main check
- CN8003, Y-Main check
- CN8005/CN8006 Buffer check
Check output voltage
Vs, Va, Vset, Vscan
,Ve
NO
Replace SMPS
YES
Go to 5.2.3 No Display
G_16380_124a.eps
190606

Figure 5-8 Power Supply Check for 42” HD w1 models 2/2

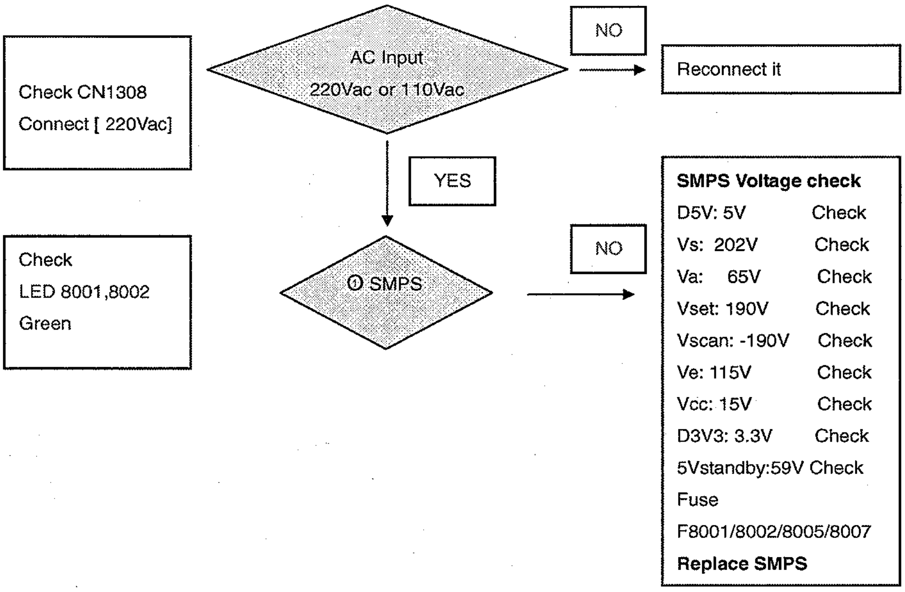

Check CN1308
Connect [220Vac]
AC Input
220Vac or 110Vac
NO
Reconnect it
YES
Check
LED 8001,8002
Green
① SMPS
NO
SMPS Voltage check
D5V: 5V Check
Vs: 202V Check
Va: 65V Check
Vset: 190V Check
Vscan: -190V Check
Ve: 115V Check
Vcc: 15V Check
D3V3: 3.3V Check
5Vstandby:59V Check
Fuse
F8001/8002/8005/8007
Replace SMPS
G_16380_125.eps
190606

Figure 5-9 Power Supply Check for 50” HD w1 models 1/2

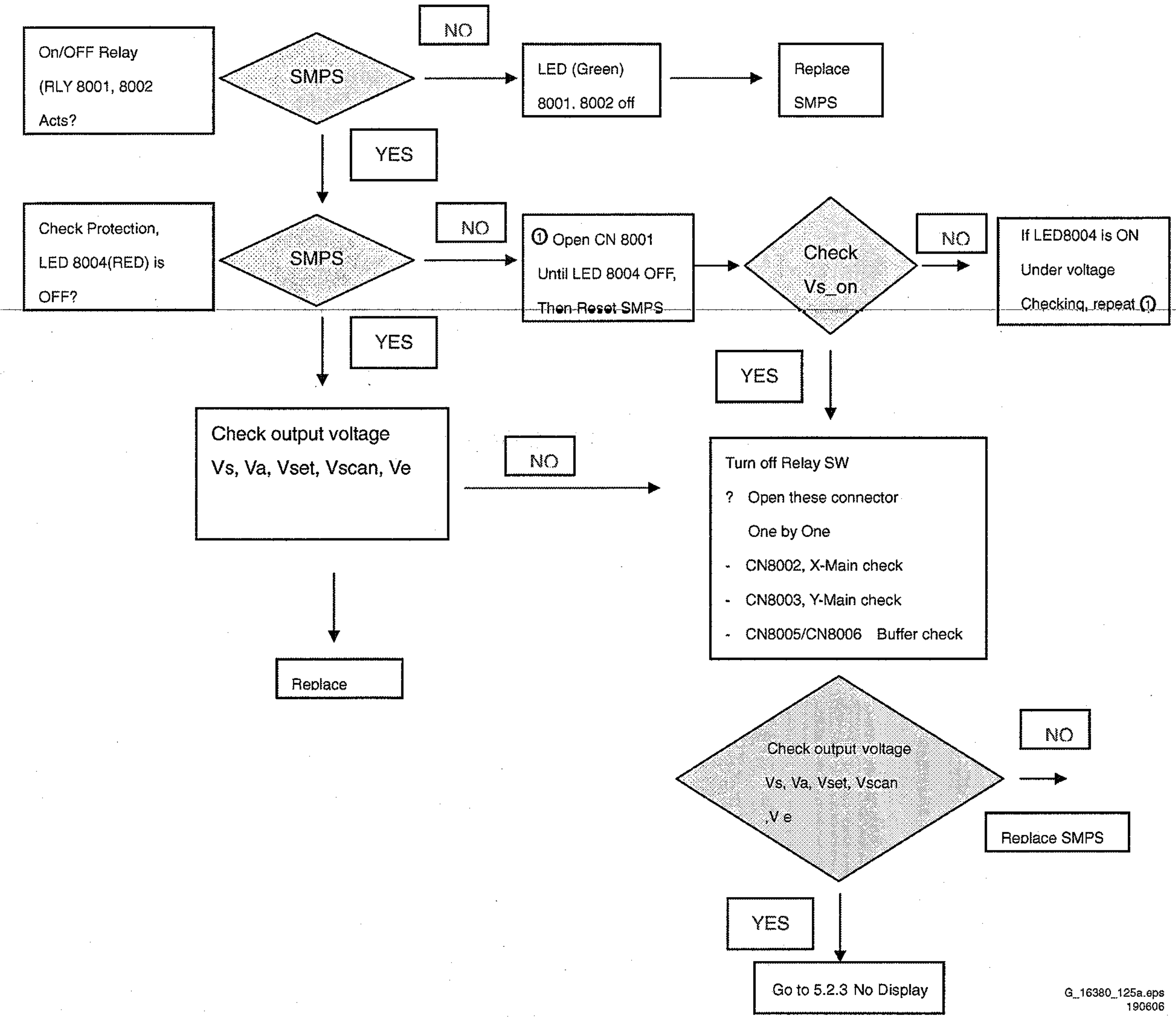

On/OFF Relay
(RLY 8001, 8002
Acts?
SMPS
NO
LED (Green)
8001, 8002 off
Replace
SMPS
YES
Check Protection,
LED 8004(RED) is
OFF?
SMPS
NO
① Open CN 8001
Until LED 8004 OFF,
Then Reset SMPS
Check
Vs_on
NO
If LED8004 is ON
Under voltage
Checking, repeat ①
YES
YES
Check output voltage
Vs, Va, Vset, Vscan, Ve
NO
Turn off Relay SW
? Open these connector
One by One
- CN8002, X-Main check
- CN8003, Y-Main check
- CN8005/CN8006 Buffer check
Replace
Check output voltage
Vs, Va, Vset, Vscan
,V e
NO
Replace SMPS
YES
Go to 5.2.3 No Display
G_16380_125a.eps
190606

Figure 5-10 Power Supply Check for 50” HD w1 models 2/2

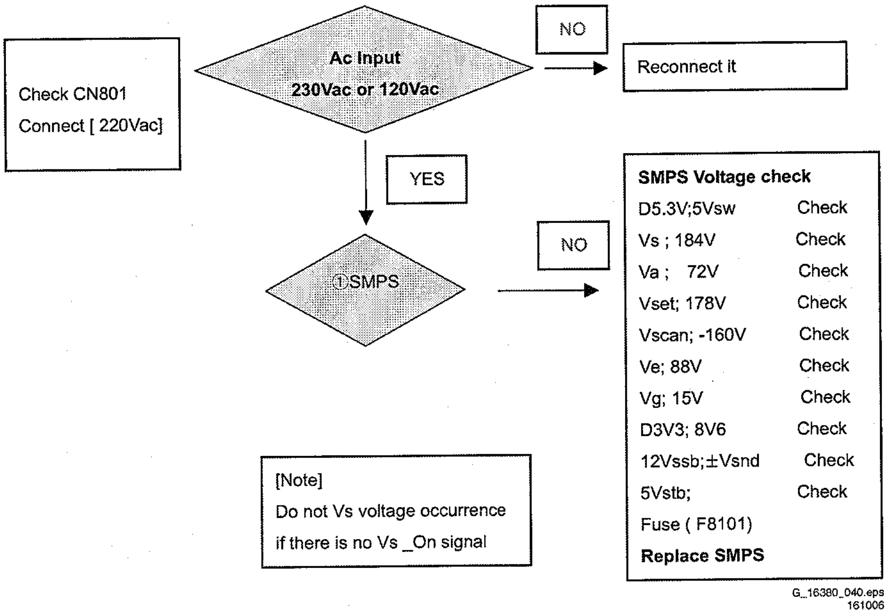

Check CN801
Connect [220Vac]
Ac Input
230Vac or 120Vac
NO
Reconnect it
YES
①SMPS
NO
SMPS Voltage check
D5.3V;5Vsw Check
Vs ; 184V Check
Va ; 72V Check
Vset; 178V Check
Vscan; -160V Check
Ve; 88V Check
Vg; 15V Check
D3V3; 8V6 Check
12Vssb;±Vsnd Check
5Vstb; Check
Fuse (F8101)
Replace SMPS
[Note]
Do not Vs voltage occurrence
if there is no Vs _On signal
G_16380_040.eps
161006

Figure 5-11 Power Supply Check for 63” HD v4 models 1/2

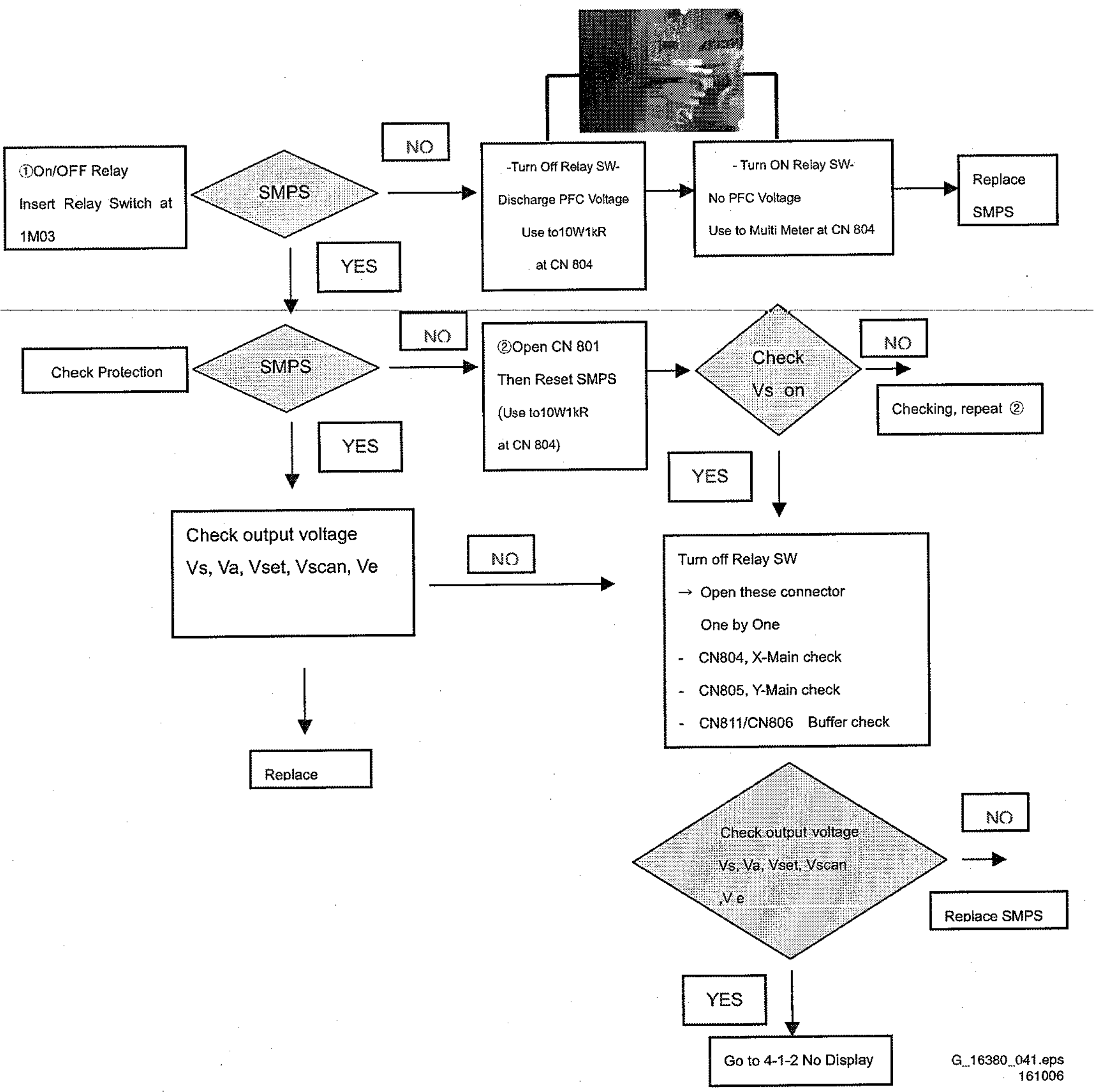
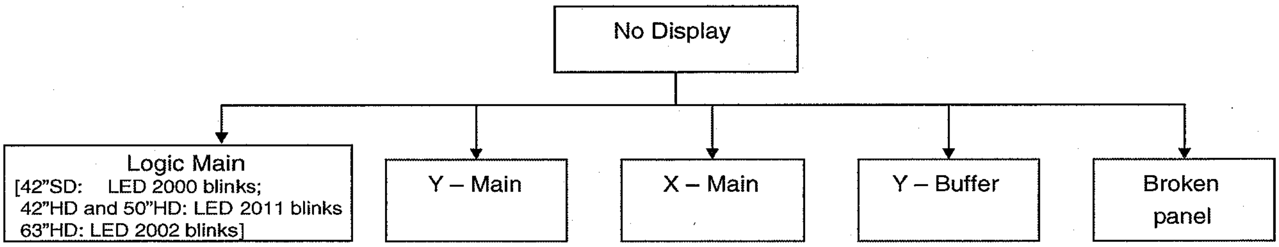

①On/OFF Relay
Insert Relay Switch at 1M03
SMPS
NO
-Turn Off Relay SW-
Discharge PFC Voltage
Use to10W1kR
at CN 804
- Turn ON Relay SW-
No PFC Voltage
Use to Multi Meter at CN 804
Replace SMPS
YES
Check Protection
SMPS
NO
②Open CN 801
Then Reset SMPS
(Use to10W1kR
at CN 804)
Check
Vs on
NO
Checking, repeat ②
YES
YES
Check output voltage
Vs, Va, Vset, Vscan, Ve
NO
Turn off Relay SW
→ Open these connector
One by One
- CN804, X-Main check
- CN805, Y-Main check
- CN811/CN806 Buffer check
Replace
Check output voltage
Vs, Va, Vset, Vscan
,V e
NO
Replace SMPS
YES
Go to 4-1-2 No Display
G_16380_041.eps
161006

Figure 5-12 Power Supply Check for 63” HD v4 models 2/2

5.2.3 No Display

(operating voltage present, but an image doesn't exist on Screen)
No Display is related with Y-MAIN, X-MAIN, Logic Main and so on.
This page shows you how to check the boards, and the following pages show you how to find the defective board.


No Display
Logic Main
[42"SD: LED 2000 blinks;
42"HD and 50"HD: LED 2011 blinks
63"HD: LED 2002 blinks]
Y – Main
X – Main
Y – Buffer
Broken panel

G_16380_127.eps
171006

Figure 5-13 Fault symptom: "No Display", general guide line

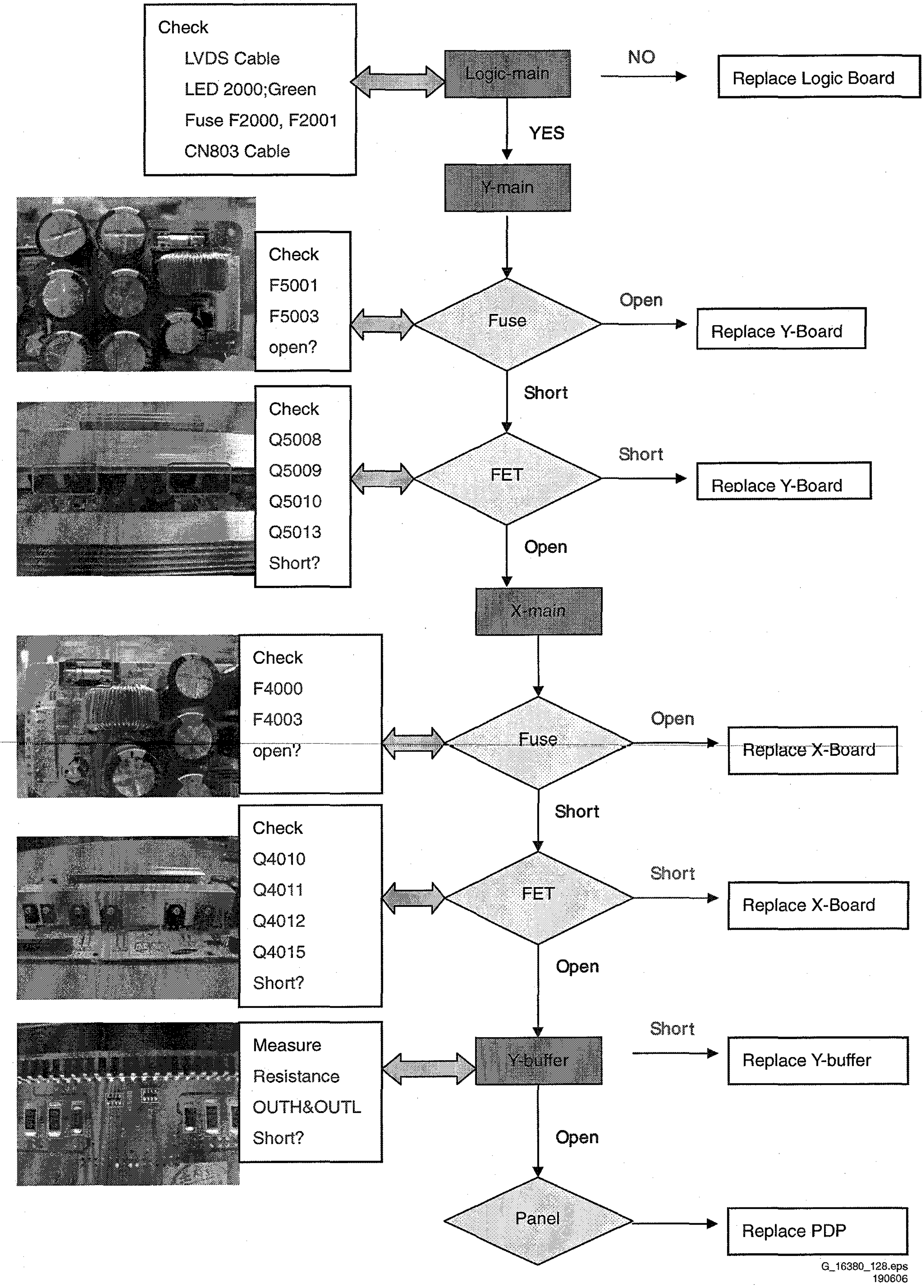

Check
LVDS Cable
LED 2000;Green
Fuse F2000, F2001
CN803 Cable
Logic-main
NO
Replace Logic Board
YES
Y-main
Check
F5001
F5003
open?
Fuse
Open
Replace Y-Board
Short
Check
Q5008
Q5009
Q5010
Q5013
Short?
FET
Short
Replace Y-Board
Open
X-main
Check
F4000
F4003
open?
Fuse
Open
Replace X-Board
Short
Check
Q4010
Q4011
Q4012
Q4015
Short?
FET
Short
Replace X-Board
Open
Measure
Resistance
OUTH&OUTL
Short?
Y-buffer
Short
Replace Y-buffer
Open
Panel
Replace PDP
G_16380_128.eps
190606

Figure 5-14 Fault symptom: "No Display", 42" SD v5

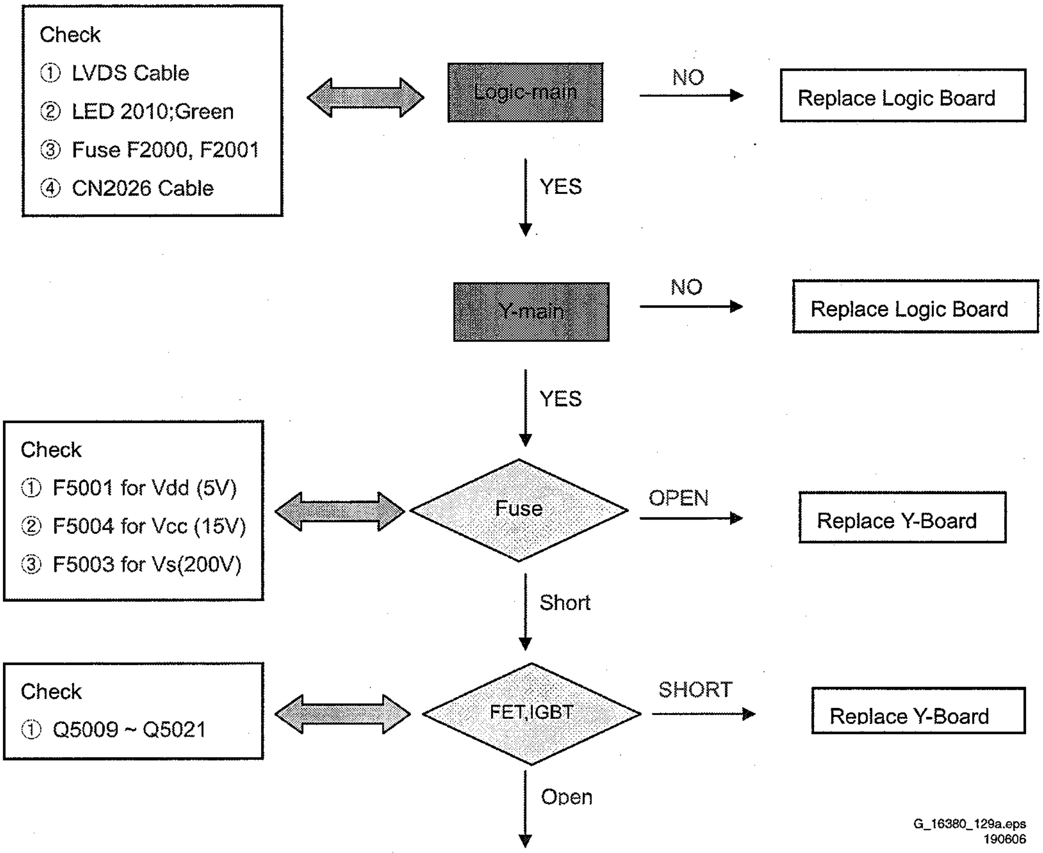
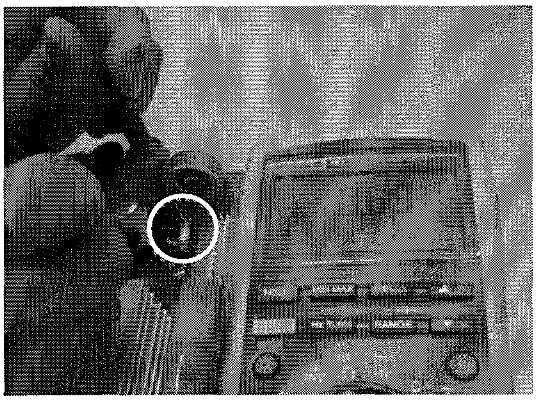
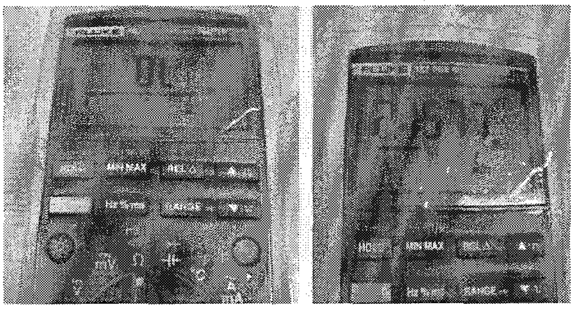
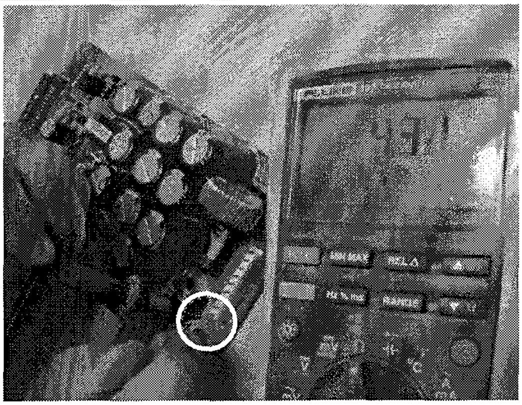
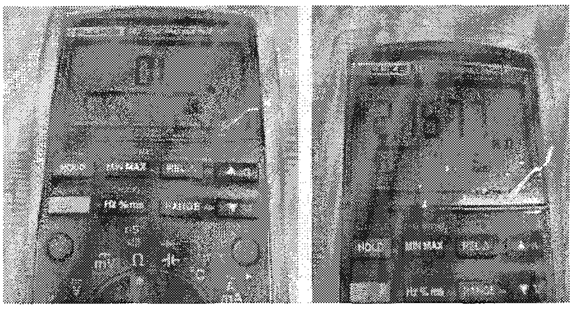
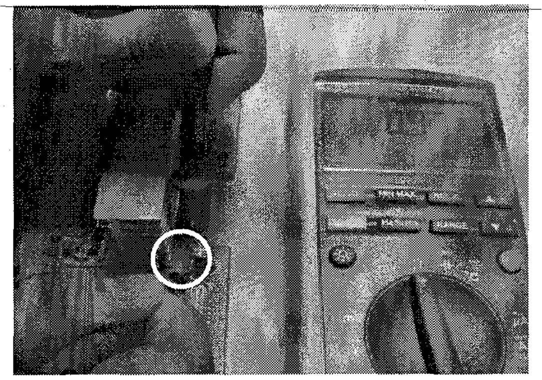
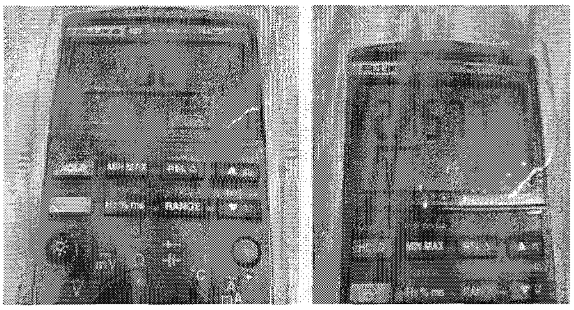

Check
① LVDS Cable
② LED 2010;Green
③ Fuse F2000, F2001
④ CN2026 Cable
Logic-main
NO
Replace Logic Board
YES
Y-main
NO
Replace Logic Board
YES
Check
① F5001 for Vdd (5V)
② F5004 for Vcc (15V)
③ F5003 for Vs(200V)
Fuse
OPEN
Replace Y-Board
Short
Check
① Q5009 ~ Q5021
FET,IGBT
SHORT
Replace Y-Board
Open
G_16380_129a.eps
190606

Figure 5-15 Fault symptom: “No Display”, 42” HD w1 1/7

Y-main Check Point

	OR 
Vs fuse (F5003) – OK (0.x ~ x.x ohm)	**Vs fuse (F5003) – OPEN** (x.x Mohm)
	OR 
15V fuse (F5004) – OK (0.x ~ x.x ohm)	**15V fuse (F5004) – OPEN** (x.x Mohm)
	OR 
5V fuse (F5001) – OK (0.x ~ x.x ohm)	**5V fuse (F5001) – OPEN** (x.x Mohm)

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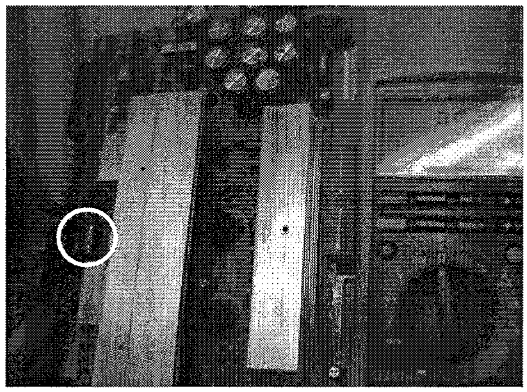
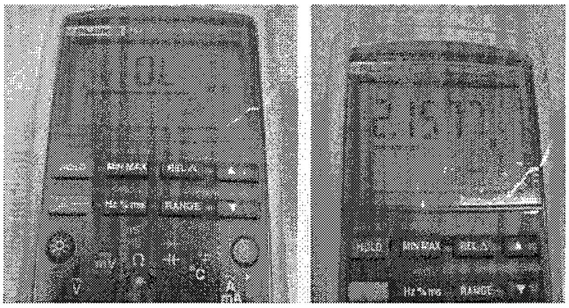
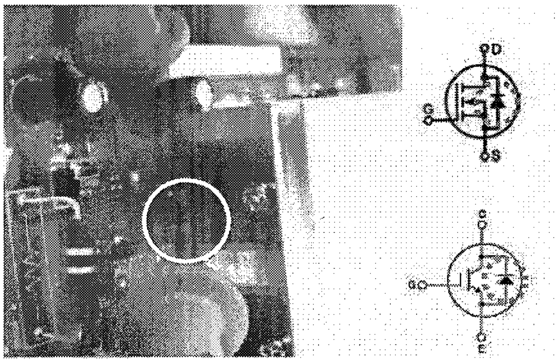
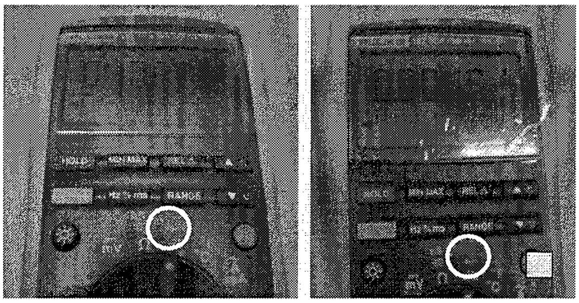
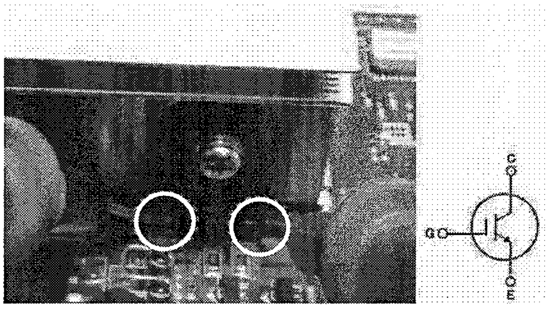
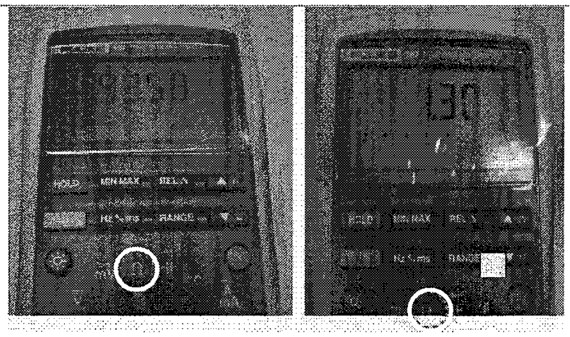
190606

Figure 5-16 Fault symptom: "No Display", 42" HD w1 2/7

	OR 
Vscan fuse (F5006) – OK (0.x ~ x.x ohm)	**Vscan fuse (F5006) – OPEN** (x.x Mohm)

IGBT, FET Check Point

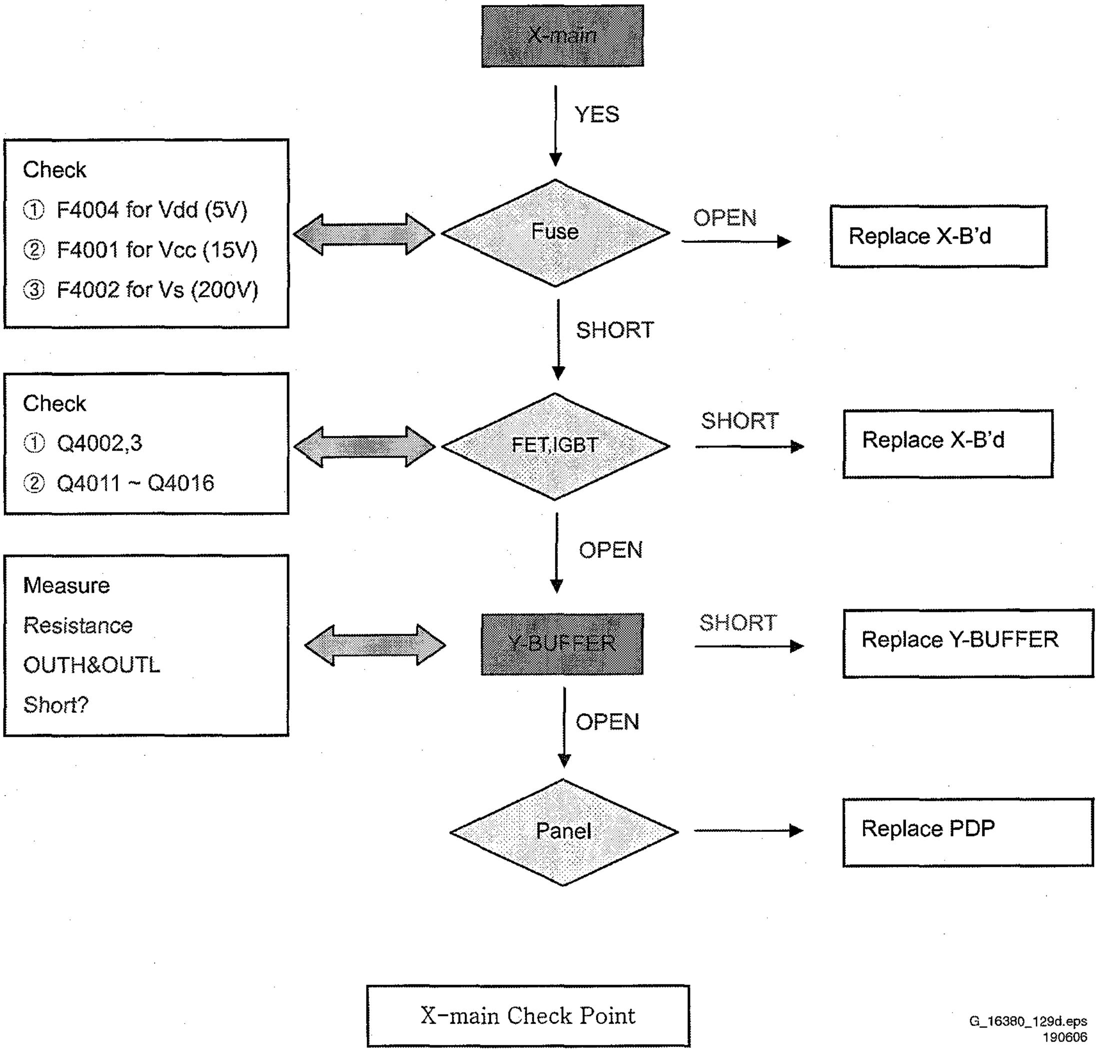
	 **OK** **Short**
FET,IGBT (contain the inner diode) **[Ys, Yg, Ypn, Yscan, Yfr, Yrr, Xs, Xg, Xe)**	**OK** (0.3 ~ 0.9 V) / **Short** (0.000 ~ 0.00x V)
	 **OK** **Short**
IGBT (do not contain the inner diode) **(Yr, Yf, Xr, Xf)**	**OK** (xx.x kohm) / **Short** (x.x ohm)

Ys(Q5013,14), Yg(Q5009,10), Ypn(Q5016,17,18), Yscan(Q5020,21), Yfr(Q5019), Yrr(Q5015), Xs(Q4002,03), Xg(Q4011,12), Xe(Q4013,14)

Yr(Q5011), Yf(Q5012), Xr(Q4016), Xf(Q4015)

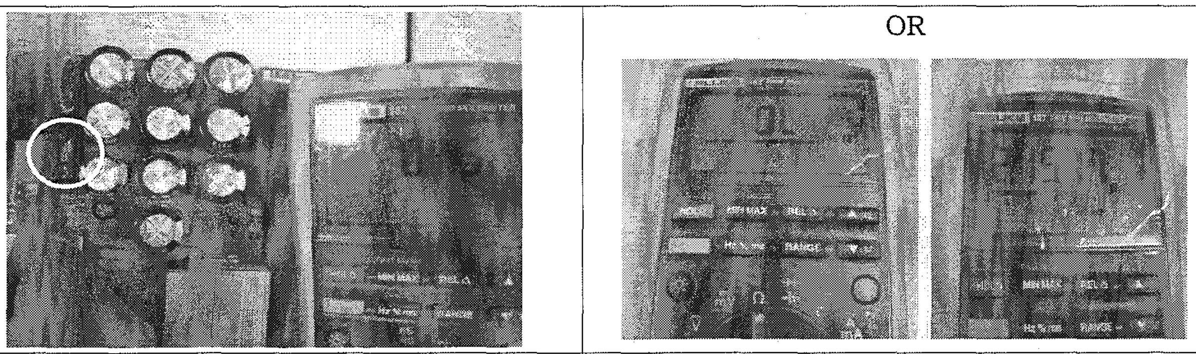
G_16380_129c.eps
190606

Figure 5-17 Fault symptom: “No Display”, 42” HD w1 3/7


X-main
YES
Check
① F4004 for Vdd (5V)
② F4001 for Vcc (15V)
③ F4002 for Vs (200V)
Fuse
OPEN
Replace X-B'd
SHORT
Check
① Q4002,3
② Q4011 ~ Q4016
FET,IGBT
SHORT
Replace X-B'd
OPEN
Measure
Resistance
OUTH&OUTL
Short?
Y-BUFFER
SHORT
Replace Y-BUFFER
OPEN
Panel
Replace PDP
X-main Check Point

G_16380_129d.eps
190606

Figure 5-18 Fault symptom: "No Display", 42" HD w1 4/7



Vs fuse (F4003) – OK (0.x ~ x.x ohm)	**Vs fuse (F4003) – OPEN** (x.x Mohm)

G_16380_129e.eps
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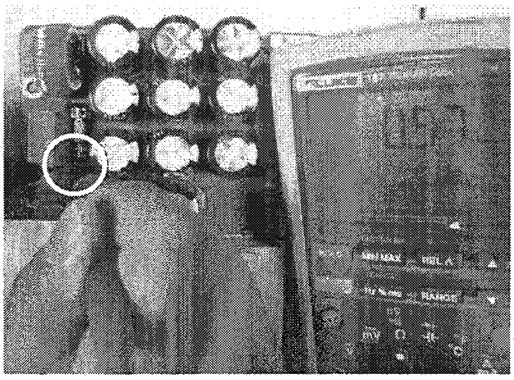
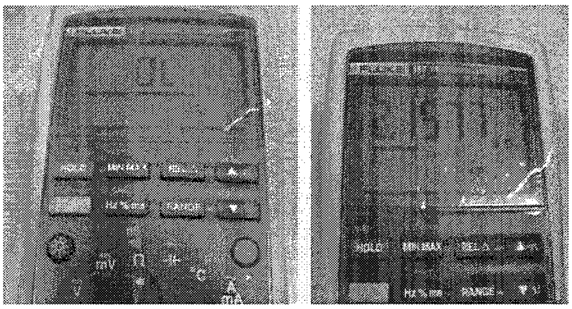
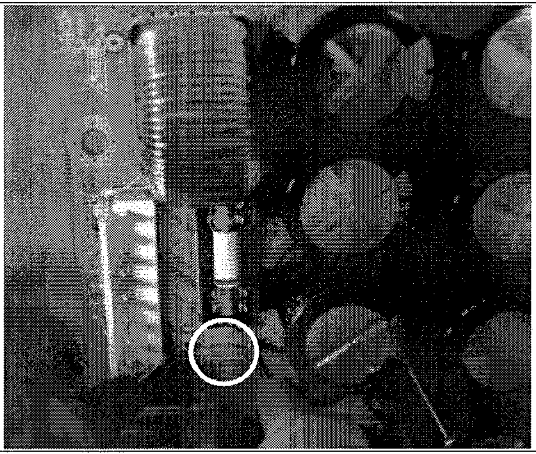
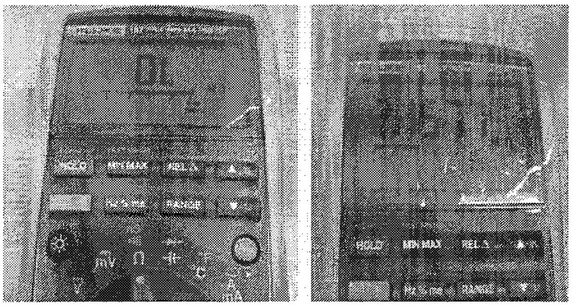
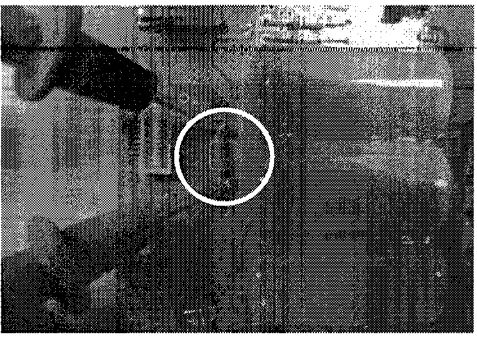
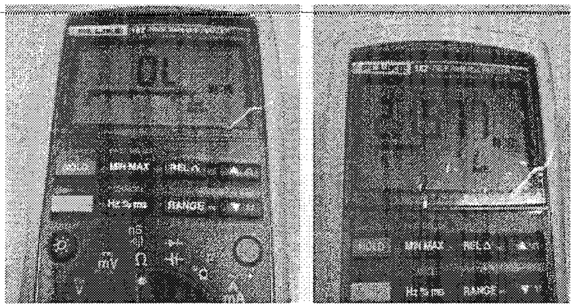
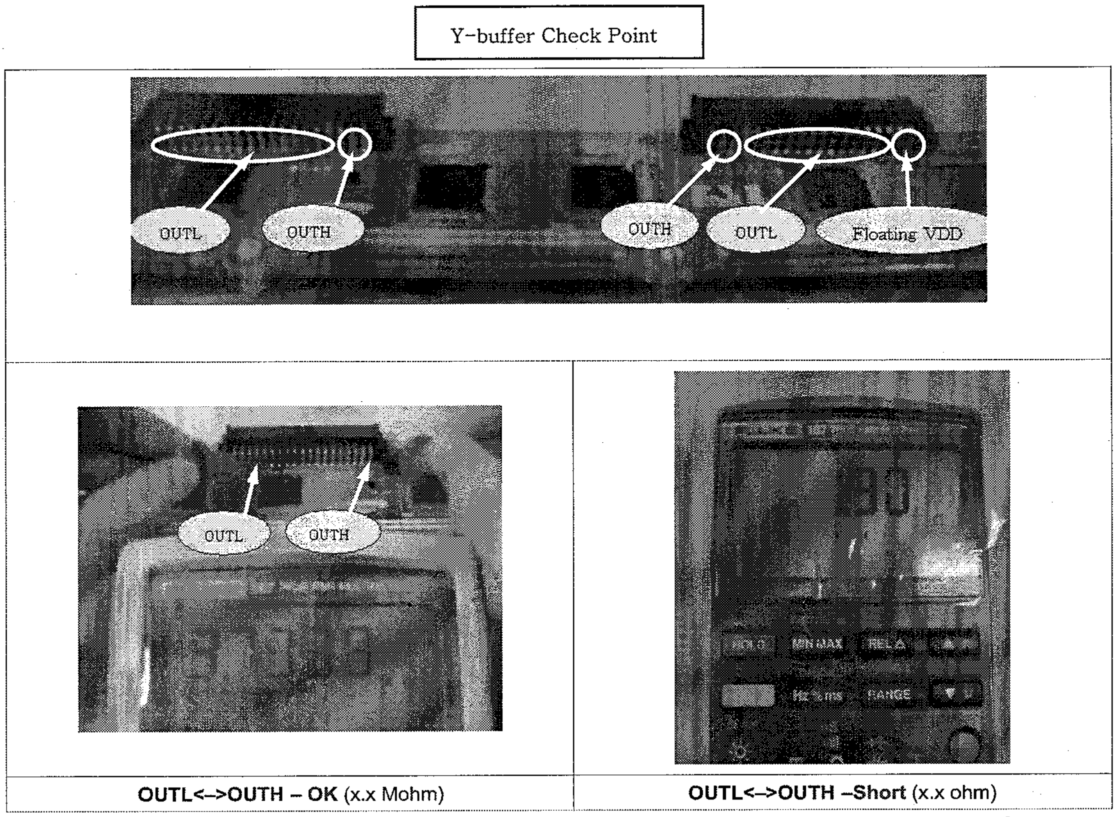
Figure 5-19 Fault symptom: "No Display", 42" HD w1 5/7

	OR 
Ve fuse (F4005) – OK (0.x ~ x.x ohm)	**Vs fuse (F4005) – OPEN** (x.x Mohm)
	OR 
15V fuse (F4001) – OK (0.x ~ x.x ohm)	**Vs fuse (F4001) – OPEN** (x.x Mohm)

	OR 
5V fuse (F4004) – OK (0.x ~ x.x ohm)	**5V fuse (F4004) – OPEN** (x.x Mohm)

G_16380_129f.eps
190606

Figure 5-20 Fault symptom: “No Display”, 42” HD w1 6/7

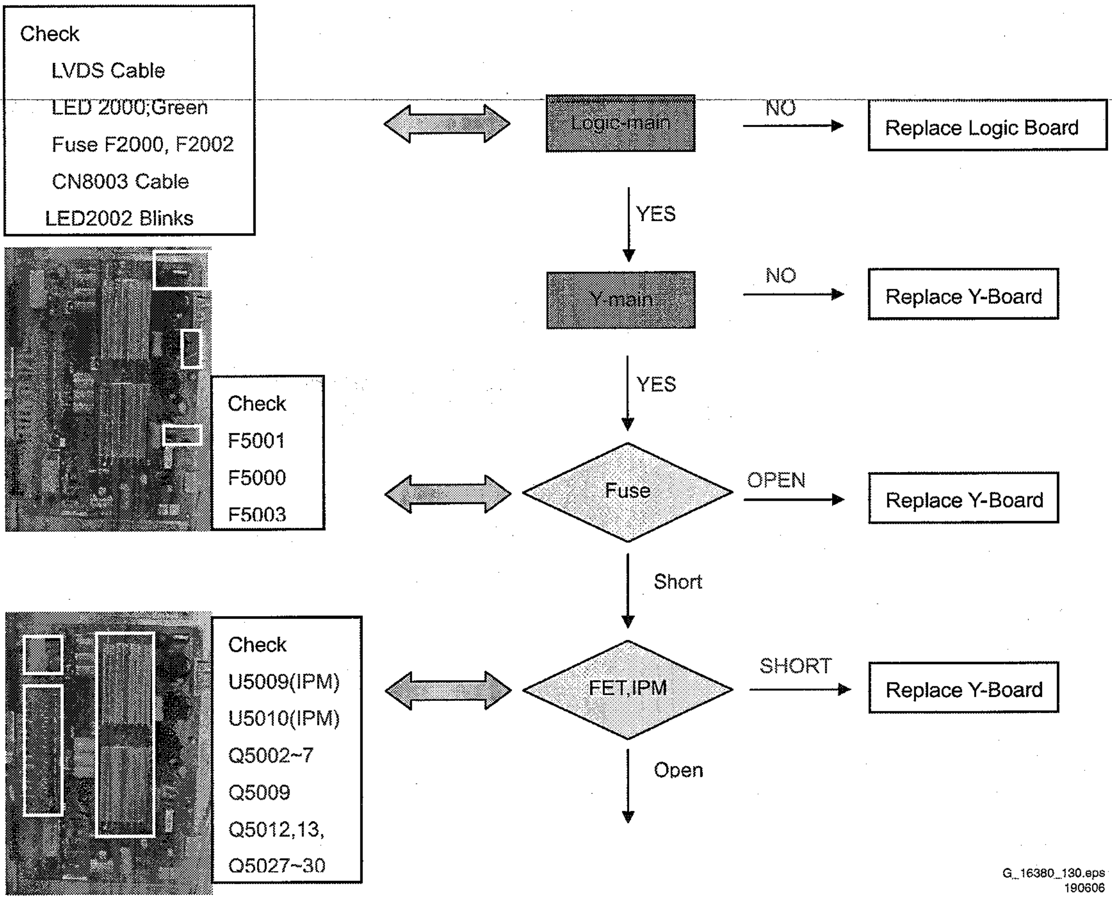

Y-buffer Check Point
OUTL
OUTH
OUTH
OUTL
Floating VDD
OUTL
OUTH

OUTL<–>OUTH – OK (x.x Mohm)

OUTL<–>OUTH –Short (x.x ohm)

G_16380_129g.eps
190606

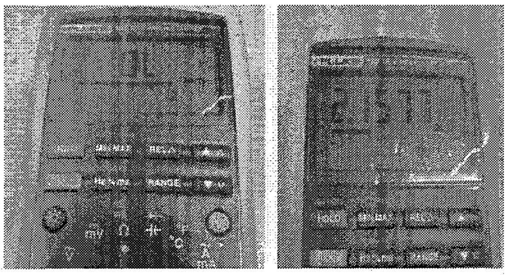
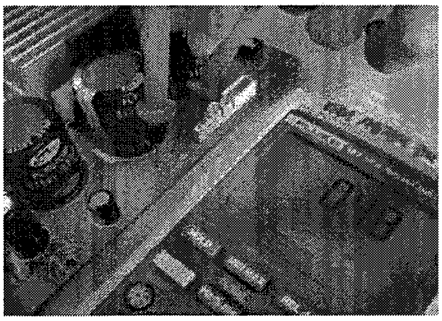
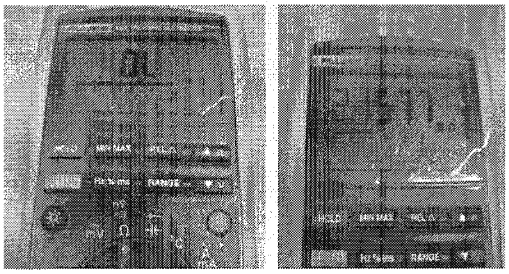
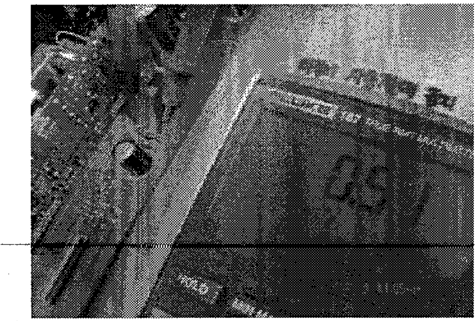
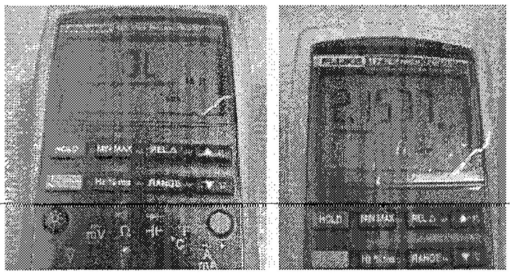
Figure 5-21 Fault symptom: “No Display”, 42” HD w1 7/7


Check
LVDS Cable
LED 2000;Green
Fuse F2000, F2002
CN8003 Cable
LED2002 Blinks
Logic-main
NO
Replace Logic Board
YES
Y-main
NO
Replace Y-Board
YES
Check
F5001
F5000
F5003
Fuse
OPEN
Replace Y-Board
Short
Check
U5009(IPM)
U5010(IPM)
Q5002~7
Q5009
Q5012,13,
Q5027~30
FET,IPM
SHORT
Replace Y-Board
Open

G_16380_130.eps
190606

Figure 5-22 Fault symptom: “No Display”, 50” HD w1 1/6

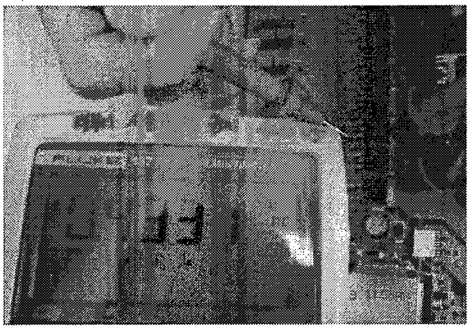
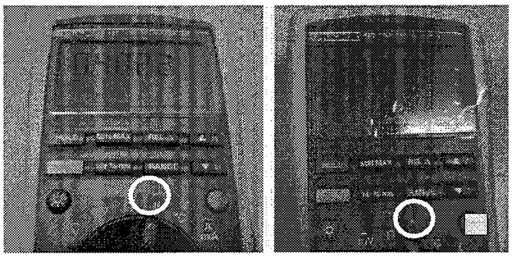
Y- main Check Point

	OR 
Vs fuse (F5003) – OK (0.x ~ x.x ohm)	Vs fuse (F5003) – OPEN (x.x Mohm)
	OR 
15V fuse (F5000) – OK (0.x ~ x.x ohm)	15V fuse (F5000) – OPEN (x.x Mohm)
	OR 
5V fuse (F5001) – OK (0.x ~ x.x ohm)	5V fuse (F5001) – OPEN (x.x Mohm)

G_16380_130a.eps
190606

Figure 5-23 Fault symptom: "No Display", 50" HD w1 2/6

IGBT, FET Check Point

	 **OK** **Short**
FET **[Ys, Yg, Ypn, Yscan, Yfr, Yrr, Xs, Xg, Xe)**	**OK** (0.3 ~ 0.9 V) / **Short** (0.000 ~ 0.00x V)

G_16380_130b.eps
190606

Figure 5-24 Fault symptom: "No Display", 50" HD w1 3/6

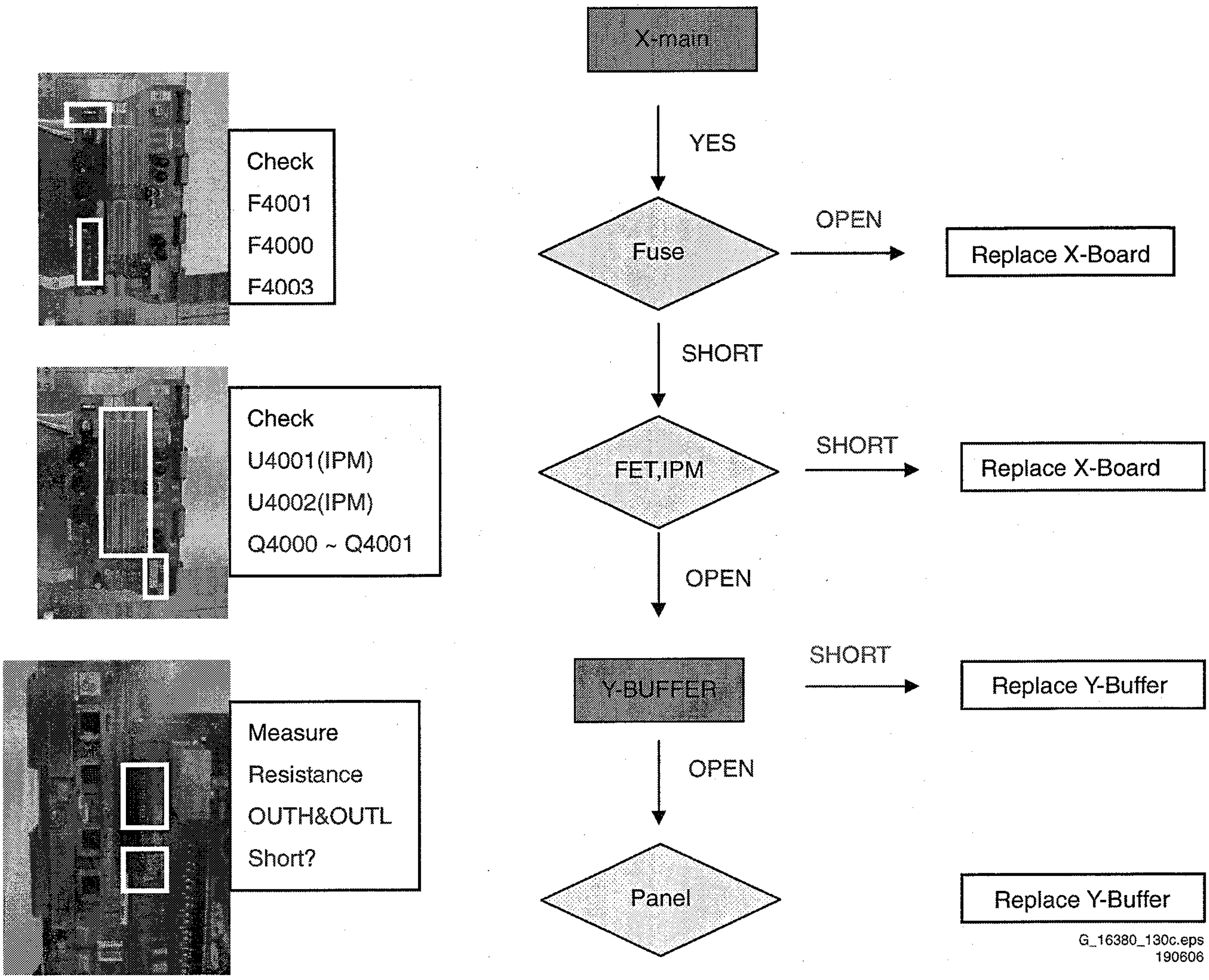
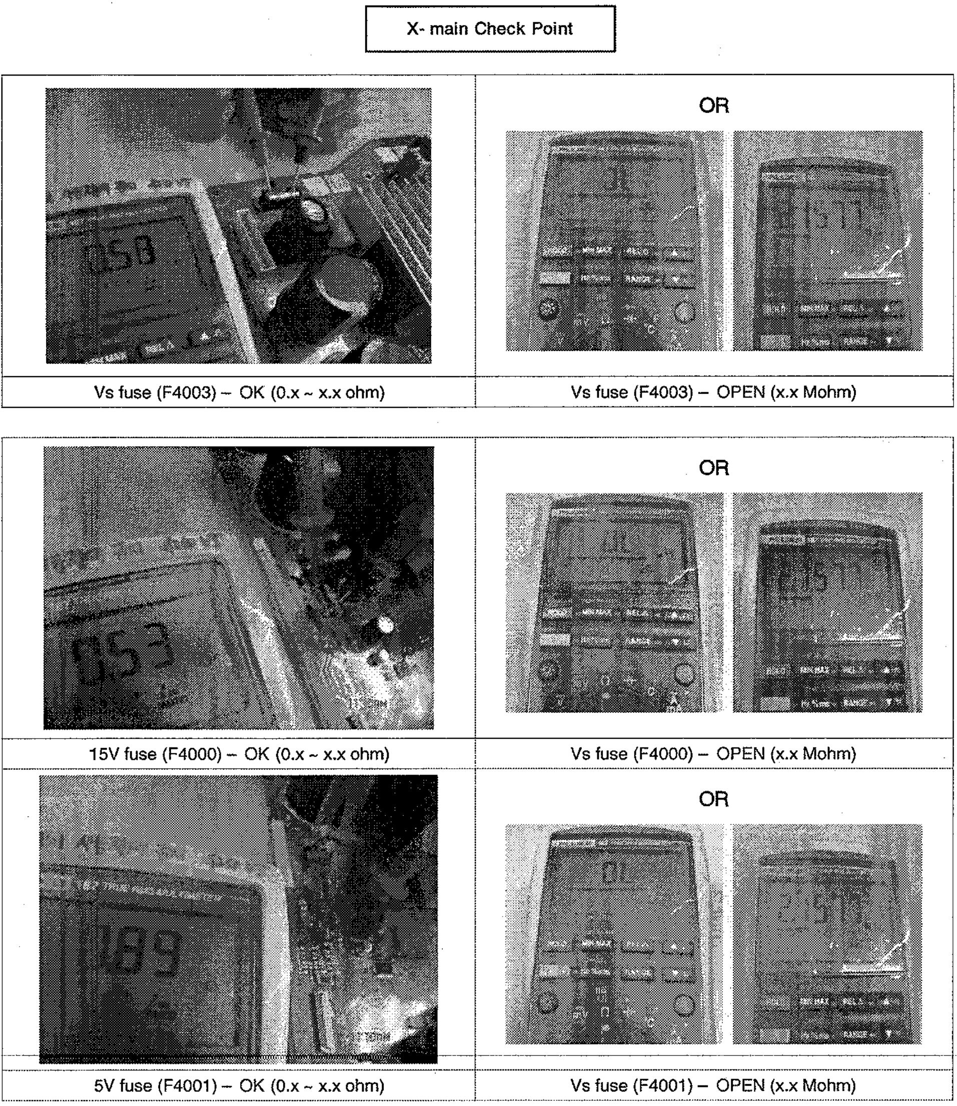

X-main
YES
Check
F4001
F4000
F4003
Fuse
OPEN
Replace X-Board
SHORT
Check
U4001(IPM)
U4002(IPM)
Q4000 ~ Q4001
FET,IPM
SHORT
Replace X-Board
OPEN
Y-BUFFER
SHORT
Replace Y-Buffer
Measure
Resistance
OUTH&OUTL
Short?
OPEN
Panel
Replace Y-Buffer
G_16380_130c.eps
190606

Figure 5-25 Fault symptom: "No Display", 50" HD w1 4/6



X- main Check Point

OR

Vs fuse (F4003) – OK (0.x ~ x.x ohm)

Vs fuse (F4003) – OPEN (x.x Mohm)

OR

15V fuse (F4000) – OK (0.x ~ x.x ohm)

Vs fuse (F4000) – OPEN (x.x Mohm)

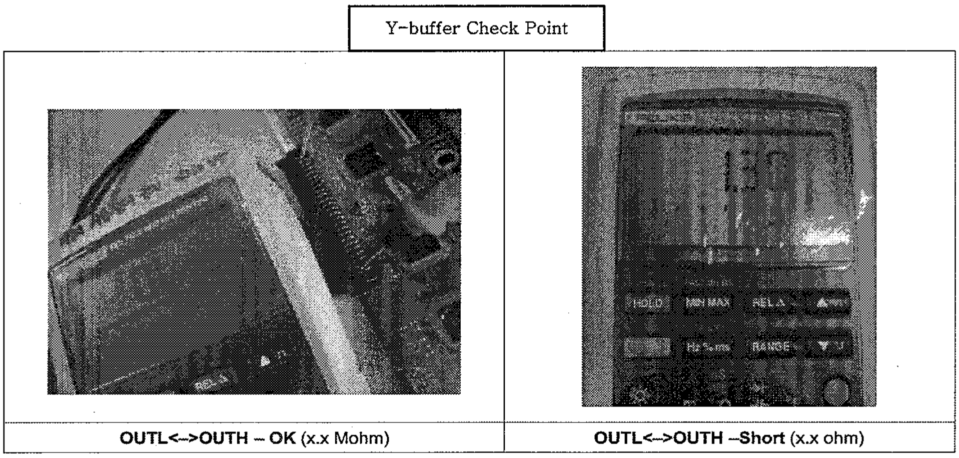
OR

5V fuse (F4001) – OK (0.x ~ x.x ohm)

Vs fuse (F4001) – OPEN (x.x Mohm)

G_16380_130d.eps
190606

Figure 5-26 Fault symptom: “No Display”, 50” HD w1 5/6



Y-buffer Check Point

OUTL<–>OUTH – OK (x.x Mohm)

OUTL<–>OUTH –Short (x.x ohm)

G_16380_130e.eps
190606

Figure 5-27 Fault symptom: “No Display”, 50” HD w1 6/6

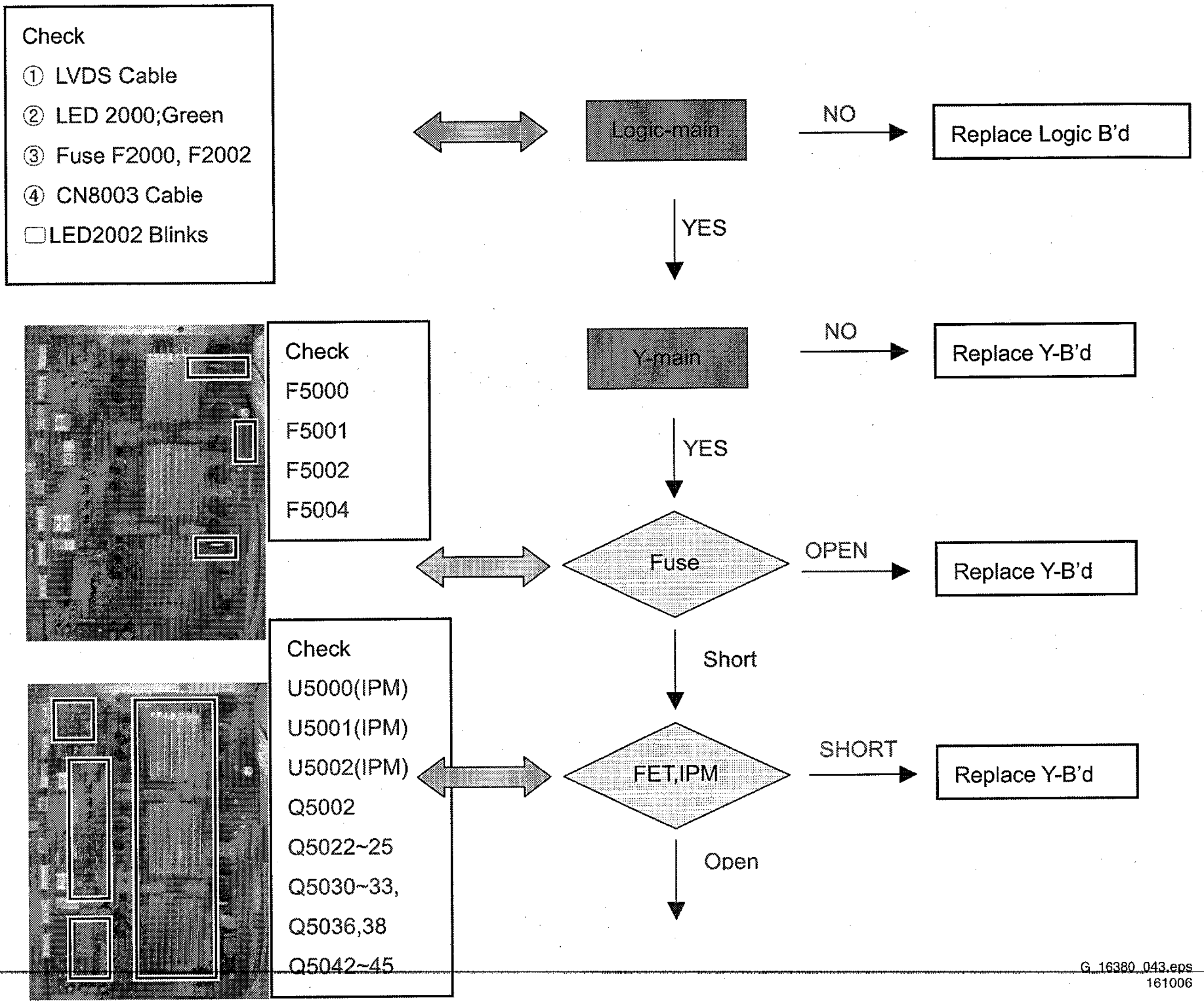
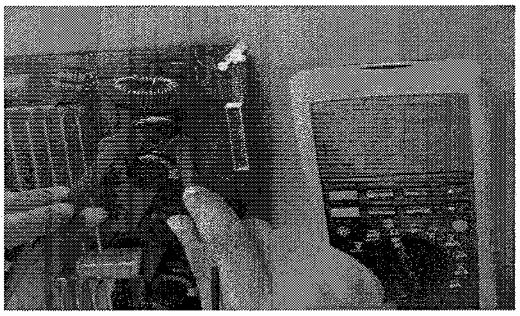

Check
① LVDS Cable
② LED 2000;Green
③ Fuse F2000, F2002
④ CN8003 Cable
▢LED2002 Blinks
Logic-main
NO
Replace Logic B'd
YES
Check
F5000
F5001
F5002
F5004
Y-main
NO
Replace Y-B'd
YES
Fuse
OPEN
Replace Y-B'd
Short
Check
U5000(IPM)
U5001(IPM)
U5002(IPM)
Q5002
Q5022~25
Q5030~33,
Q5036,38
Q5042~45
FET,IPM
SHORT
Replace Y-B'd
Open
G_16380_043.eps
161006

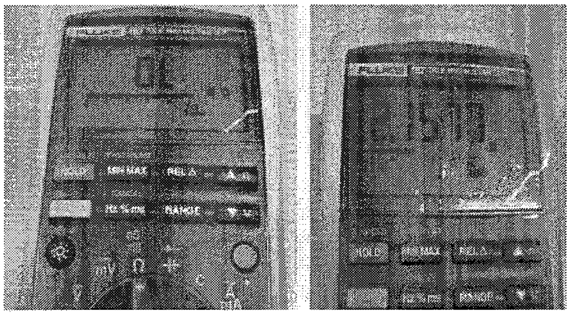
Figure 5-28 Fault symptom: "No Display", 63" HD v4 1/6

Y-main Check Point

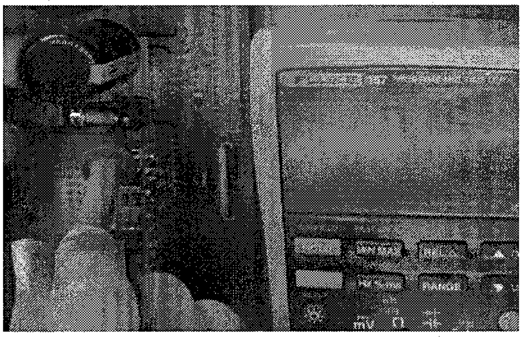


Vs fuse (F5002) – OK (0.x ~ x.x ohm)

OR

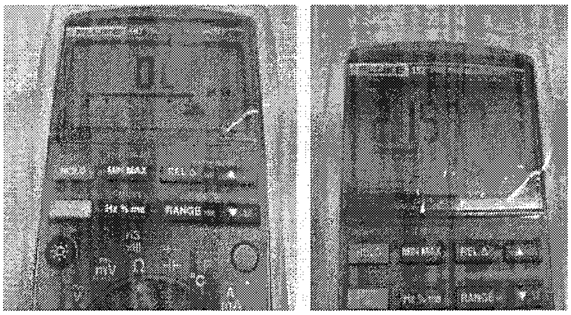


Vs fuse (F5002) – OPEN (x.x Mohm)

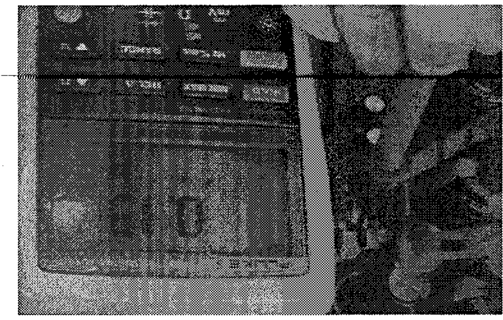


Vs fuse (F5004) – OK (0.x ~ x.x ohm)

OR

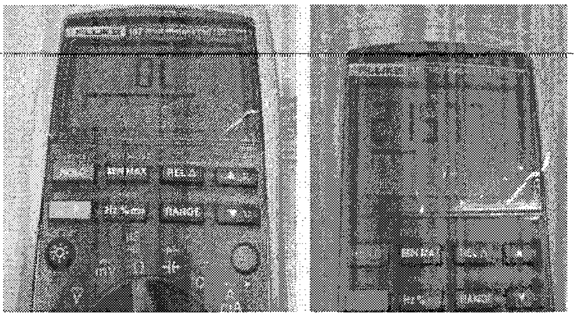


Vs fuse (F5004) – OPEN (x.x Mohm)

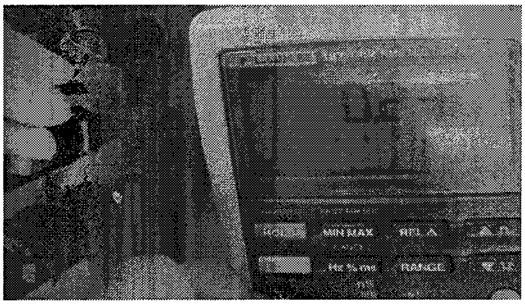


15V fuse (F5001) – OK (0.x ~ x.x ohm)

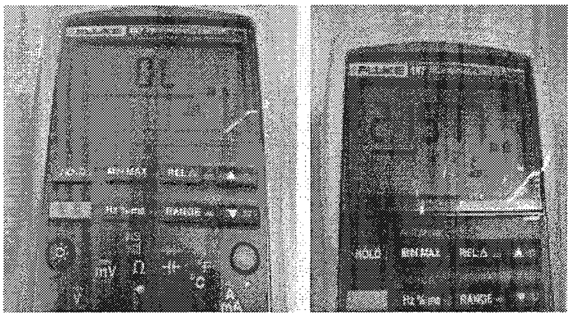
OR



15V fuse (F5001) – OPEN (x.x Mohm)



5V fuse (F5000) – OK (0.x ~ x.x ohm)

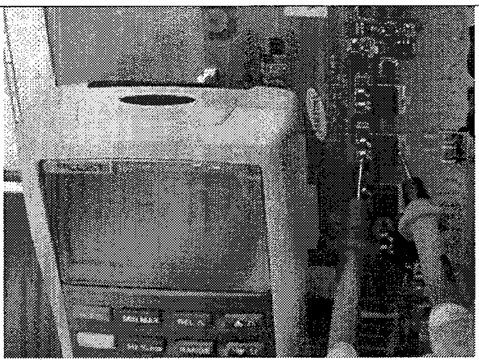
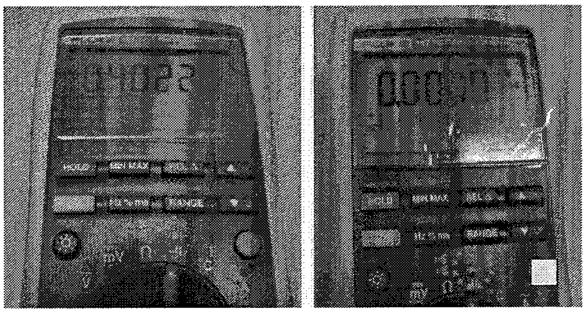
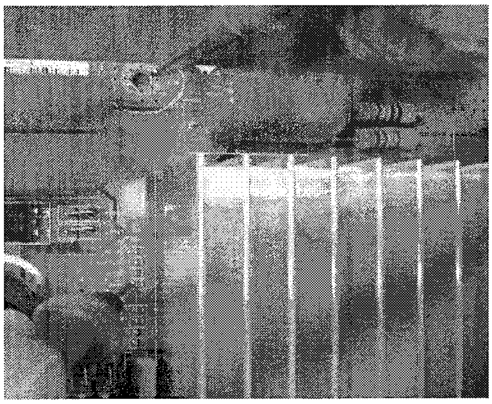
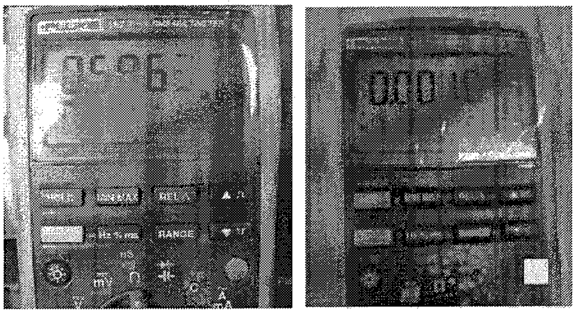


5V fuse (F5000) – OPEN (x.x Mohm)

G_16380_044.eps
161006

Figure 5-29 Fault symptom: "No Display", 63" HD v4 2/6

FET,IPM Check Point

	 **OK** **Short**
FET **[Ys, Yg, Ypn, Yscan, Yfr, Yrr, Xs, Xg, Xe)**	**OK** (0.3 ~ 0.9 V) / **Short** (0.000 ~ 0.00x V)
	 **OK** **Short**
IPM	**OK** (X.X Mohm) / **Short** (0.000 ~ 0.00x ohm)

G_16380_045.eps
161006

Figure 5-30 Fault symptom: “No Display”, 63” HD v4 3/6

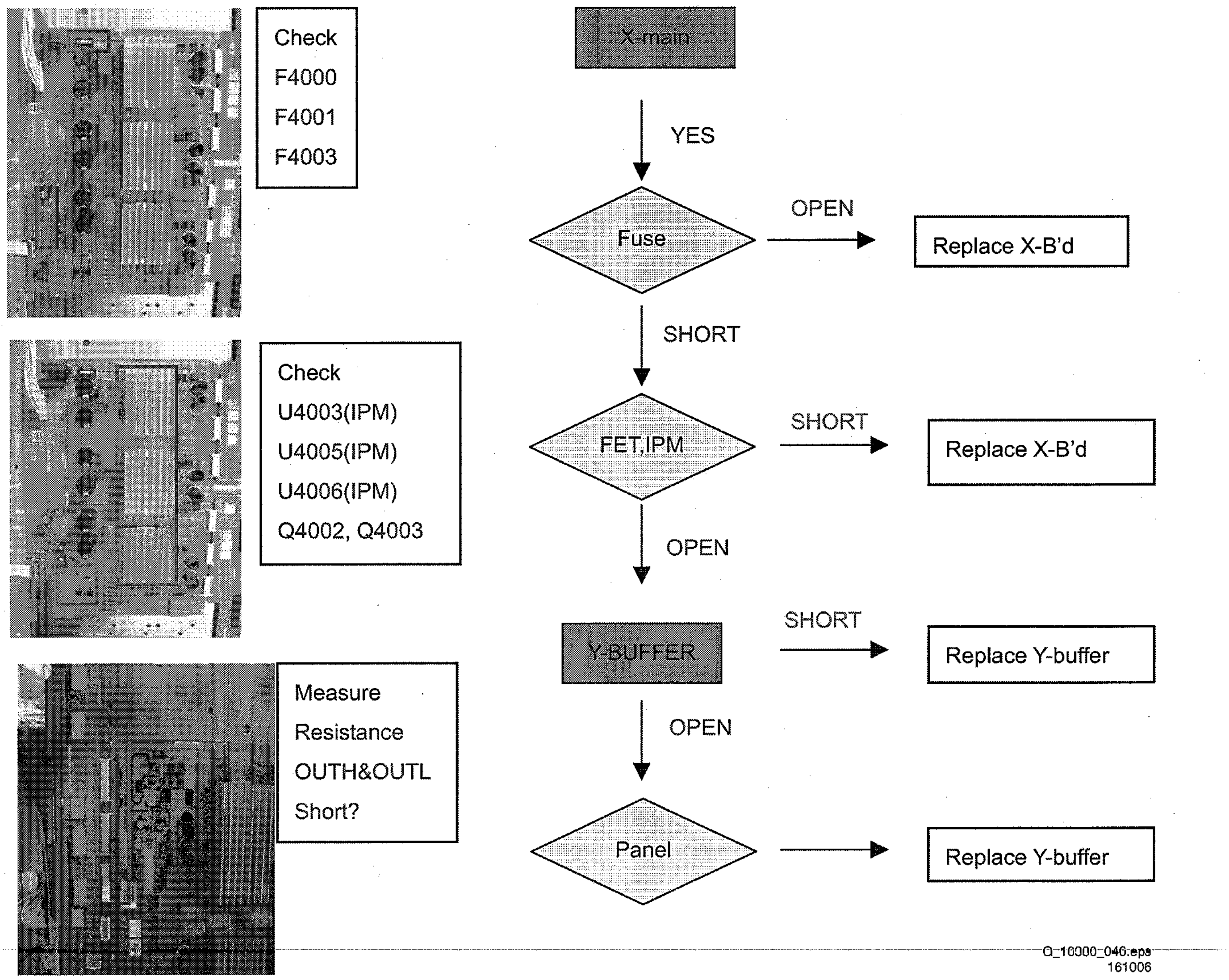
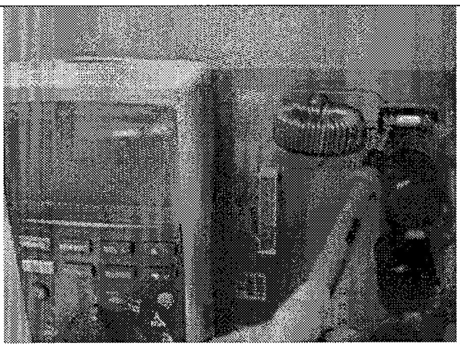
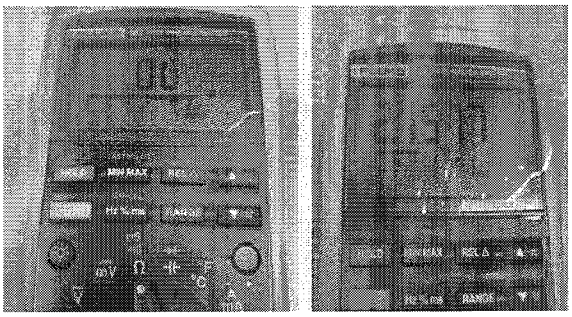
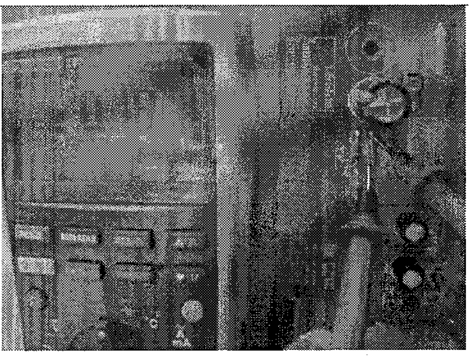
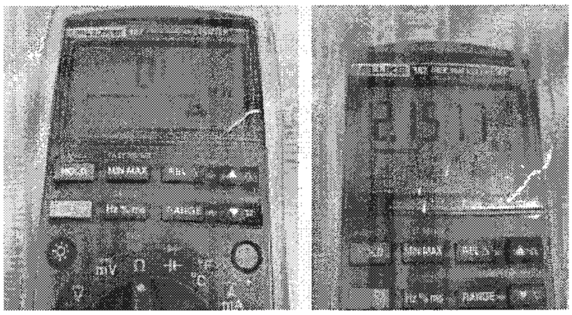
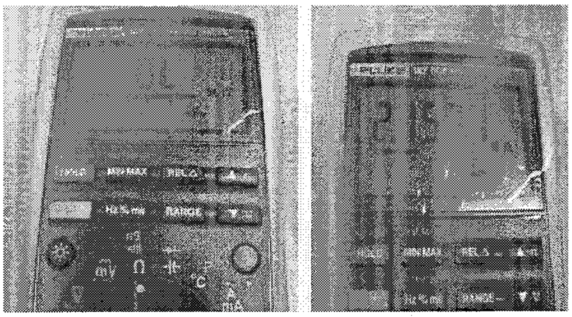

Check
F4000
F4001
F4003
Check
U4003(IPM)
U4005(IPM)
U4006(IPM)
Q4002, Q4003
Measure
Resistance
OUTH&OUTL
Short?
X-main
YES
Fuse
OPEN
Replace X-B'd
SHORT
FET,IPM
SHORT
Replace X-B'd
OPEN
Y-BUFFER
SHORT
Replace Y-buffer
OPEN
Panel
Replace Y-buffer
Q_16000_046.eps
161006

Figure 5-31 Fault symptom: “No Display”, 63” HD v4 4/6

X-main Check Point

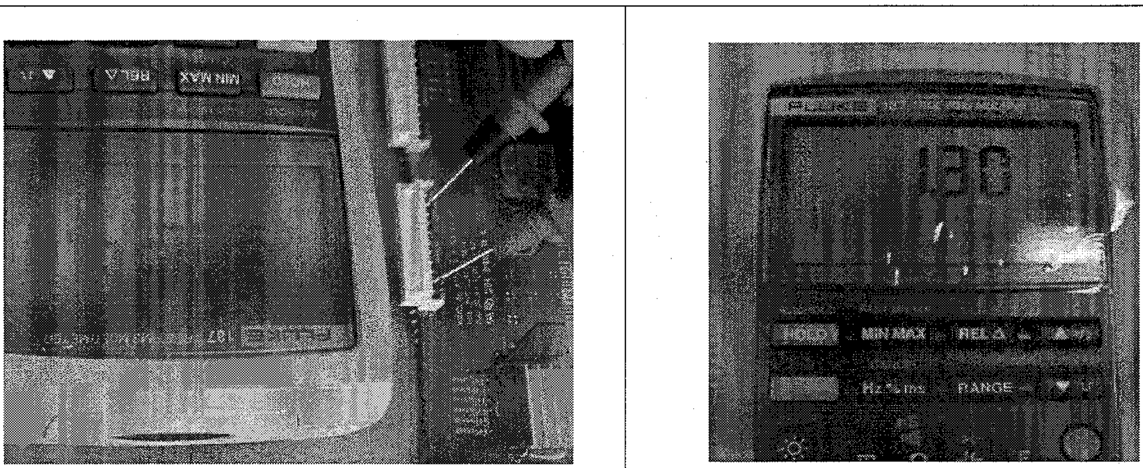
	OR 
Vs fuse (F4003) – OK (0.x ~ x.x ohm)	**Vs fuse (F4003) – OPEN** (x.x Mohm)

	OR 
15V fuse (F4001) – OK (0.x ~ x.x ohm)	**15V fuse (F4001) – OPEN** (x.x Mohm)
	OR 
5V fuse (F4000) – OK (0.x ~ x.x ohm)	**Vs fuse (F4000) – OPEN** (x.x Mohm)

G_16380_047.eps
161006

Figure 5-32 Fault symptom: "No Display", 63" HD v4 5/6

Y-buffer Check Point



OUTL<–>OUTH – OK (x.x Mohm)	**OUTL<–>OUTH –Short** (x.x ohm)

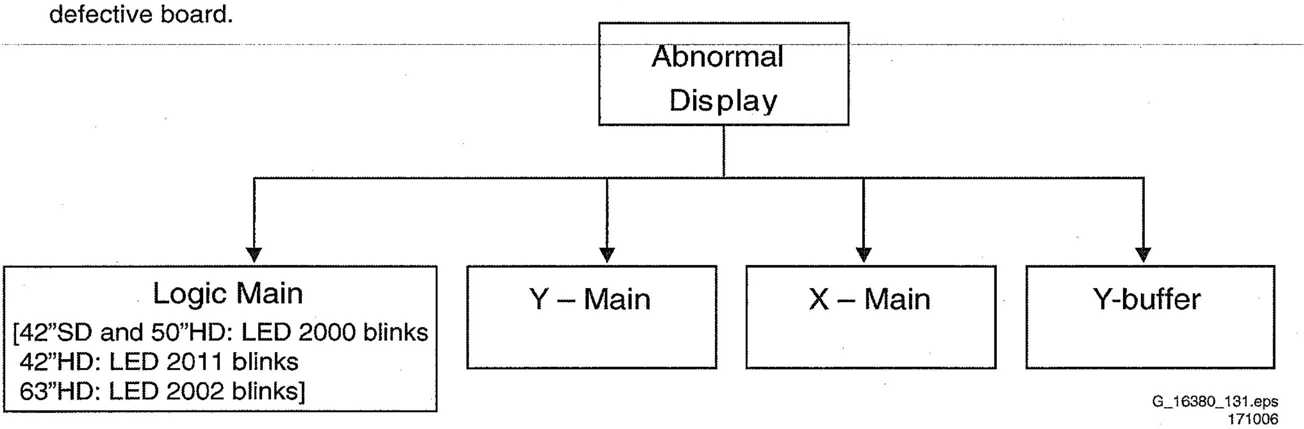
G_16380_048.eps
161006

Figure 5-33 Fault symptom: “No Display”, 63” HD v4 6/6

5.2.4 Abnormal display

(Abnormal Image is on Screen (except abnormality in Sustain or Address)

-> Abnormal Display is related with Y-MAIN, X-MAIN, Logic Main, Y-buffer and so on. This page shows you how to check the boards, and the following pages show you how to find the defective board.


Abnormal Display
Logic Main
[42”SD and 50”HD: LED 2000 blinks
42”HD: LED 2011 blinks
63”HD: LED 2002 blinks]
Y – Main
X – Main
Y-buffer

G_16380_131.eps
171006

Figure 5-34 Fault symptom: “Abnormal Display”, general guide line

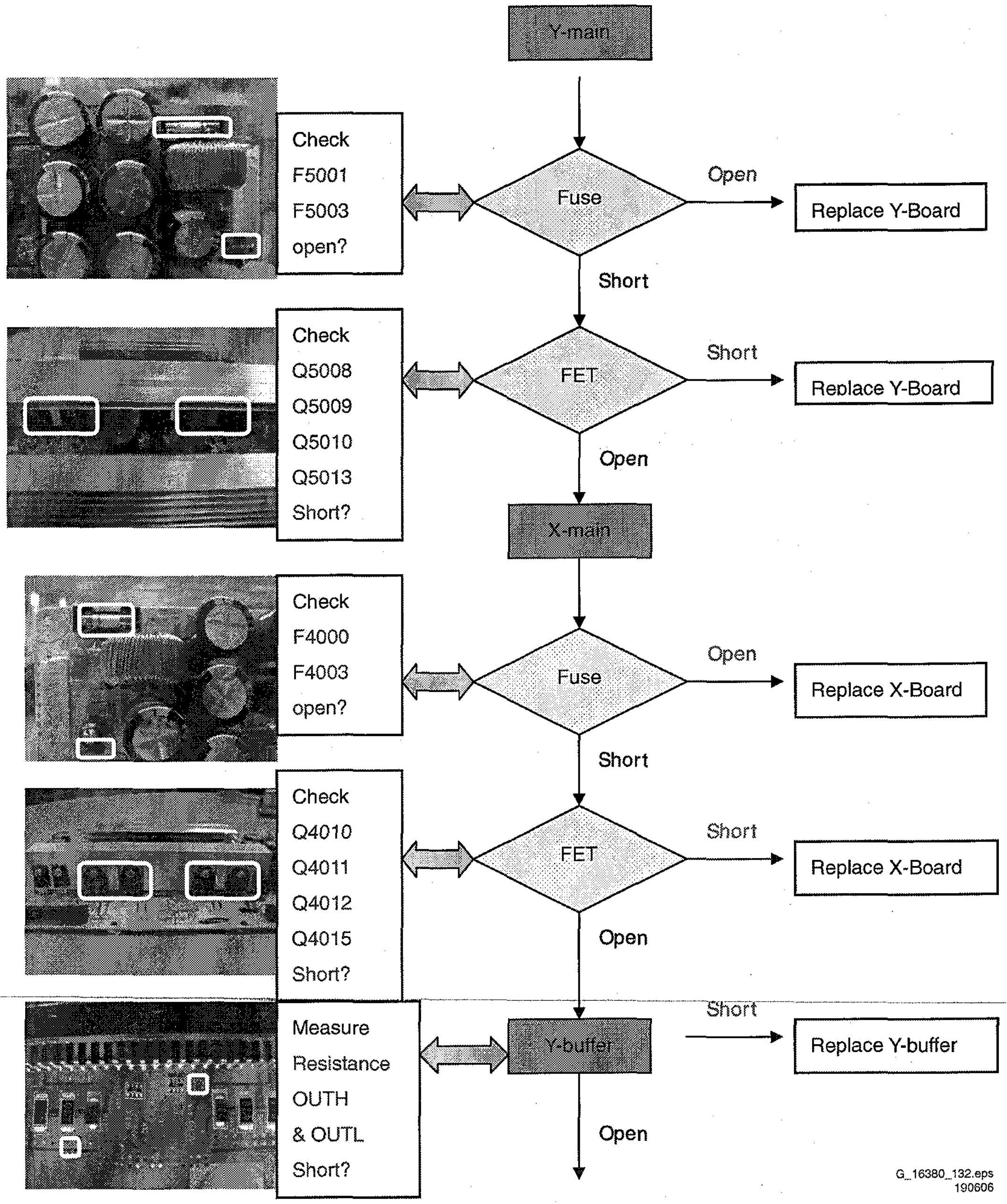

Y-main
Check
F5001
F5003
open?
Fuse
Open
Replace Y-Board
Short
Check
Q5008
Q5009
Q5010
Q5013
Short?
FET
Short
Replace Y-Board
Open
X-main
Check
F4000
F4003
open?
Fuse
Open
Replace X-Board
Short
Check
Q4010
Q4011
Q4012
Q4015
Short?
FET
Short
Replace X-Board
Open
Measure
Resistance
OUTH
& OUTL
Short?
Y-buffer
Short
Replace Y-buffer
Open
G_16380_132.eps
190606

Figure 5-35 Fault symptom: “Abnormal Display” 42” SD v5 1/2

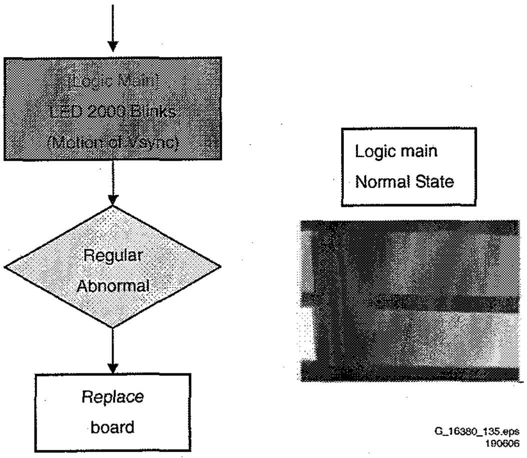
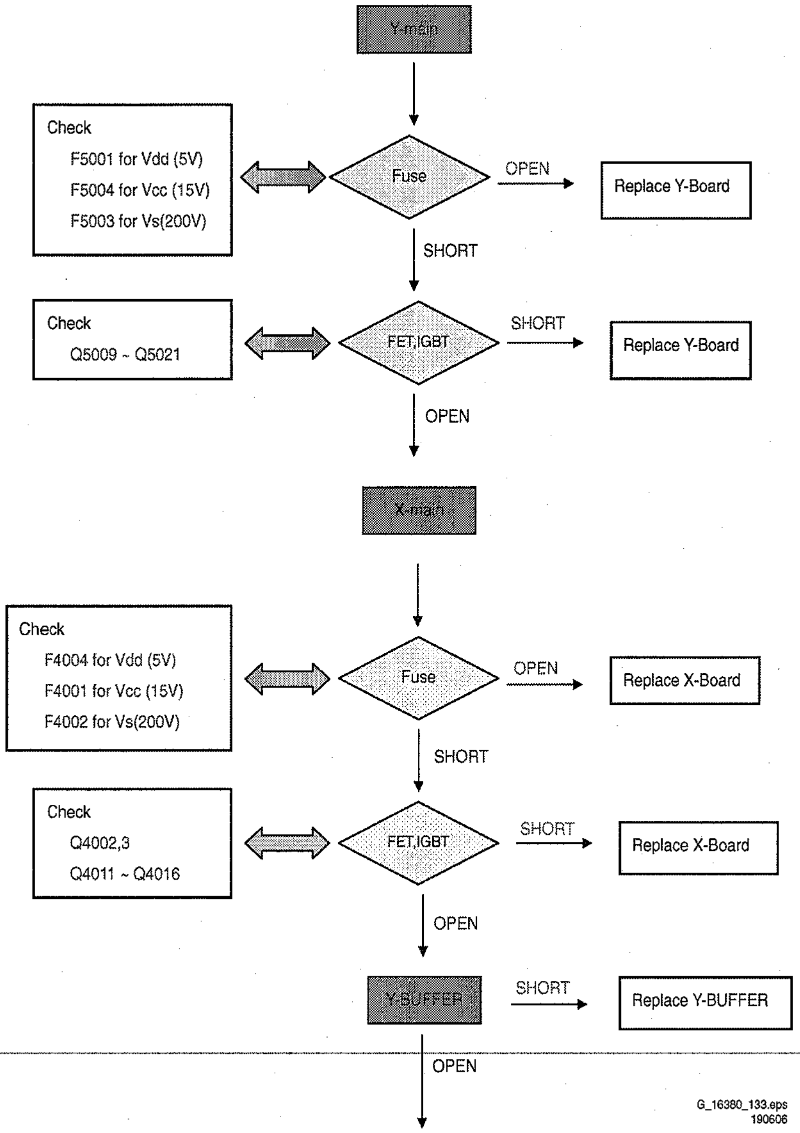
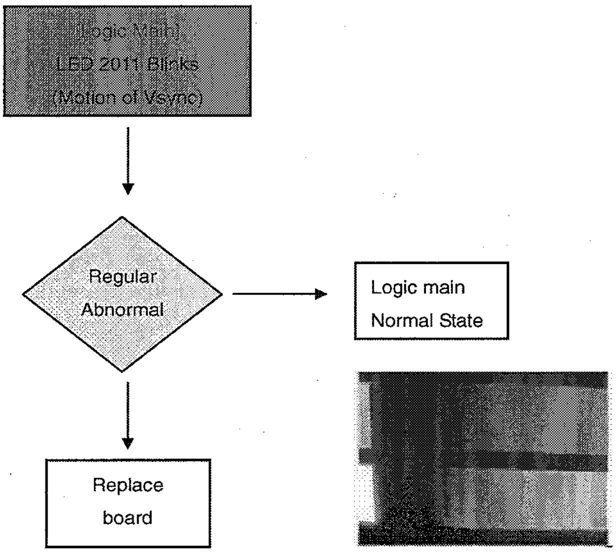

[Logic Main]
LED 2000 Blinks
(Motion of Vsync)
Regular
Abnormal
Replace
board
Logic main
Normal State
G_16380_135.eps
190606

Figure 5-36 Fault symptom: “Abnormal Display” 42” SD v5 2/2


Y-main
Check
F5001 for Vdd (5V)
F5004 for Vcc (15V)
F5003 for Vs(200V)
Fuse
OPEN
Replace Y-Board
SHORT
Check
Q5009 ~ Q5021
FET,IGBT
SHORT
Replace Y-Board
OPEN
X-main
Check
F4004 for Vdd (5V)
F4001 for Vcc (15V)
F4002 for Vs(200V)
Fuse
OPEN
Replace X-Board
SHORT
Check
Q4002,3
Q4011 ~ Q4016
FET,IGBT
SHORT
Replace X-Board
OPEN
Y-BUFFER
SHORT
Replace Y-BUFFER
OPEN

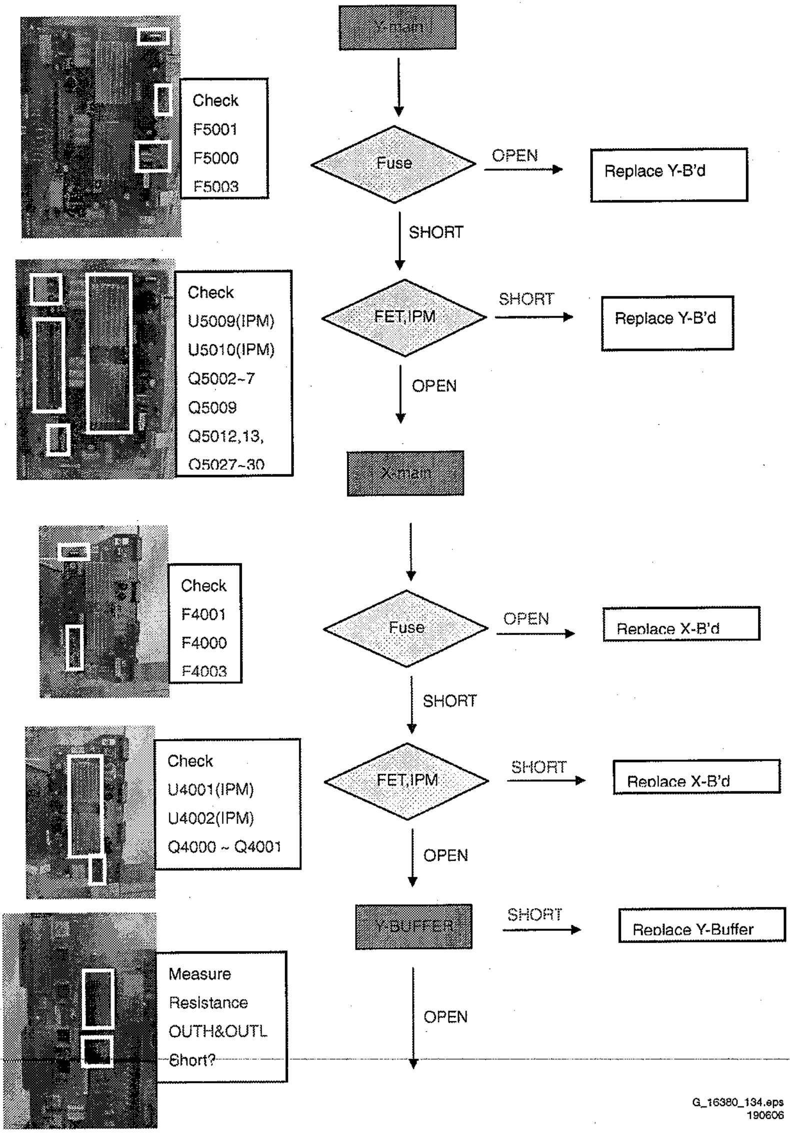
G_16380_133.eps
190606

Figure 5-37 Fault symptom: “Abnormal Display” 42” HD w1 1/2


(Logic Main)
LED 2011 Blinks
(Motion of Vsync)
Regular
Abnormal
Logic main
Normal State
Replace
board

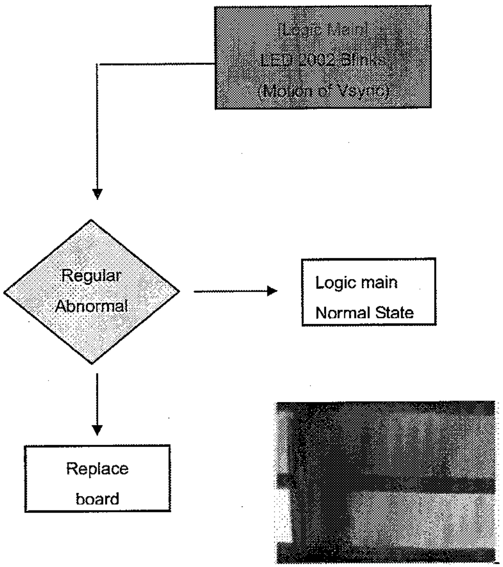
G_16380_136.eps
190606

Figure 5-38 Fault symptom: “Abnormal Display” 42” HD w1 2/2


Y-main
Check
F5001
F5000
F5003
Fuse
OPEN
Replace Y-B'd
SHORT
Check
U5009(IPM)
U5010(IPM)
Q5002~7
Q5009
Q5012,13,
Q5027~30
FET,IPM
SHORT
Replace Y-B'd
OPEN
X-main
Check
F4001
F4000
F4003
Fuse
OPEN
Replace X-B'd
SHORT
Check
U4001(IPM)
U4002(IPM)
Q4000 ~ Q4001
FET,IPM
SHORT
Replace X-B'd
OPEN
Y-BUFFER
SHORT
Replace Y-Buffer
Measure
Resistance
OUTH&OUTL
Short?
OPEN

G_16380_134.eps
190606

Figure 5-39 Fault symptom: "Abnormal Display" 50" HD w1 1/2


[Logic Main]
LED 2002 Blinks
(Motion of Vsync)
Regular
Abnormal
Logic main
Normal State
Replace
board

G_16380_137.eps
190606

Figure 5-40 Fault symptom: "Abnormal Display" 50" HD w1 2/2

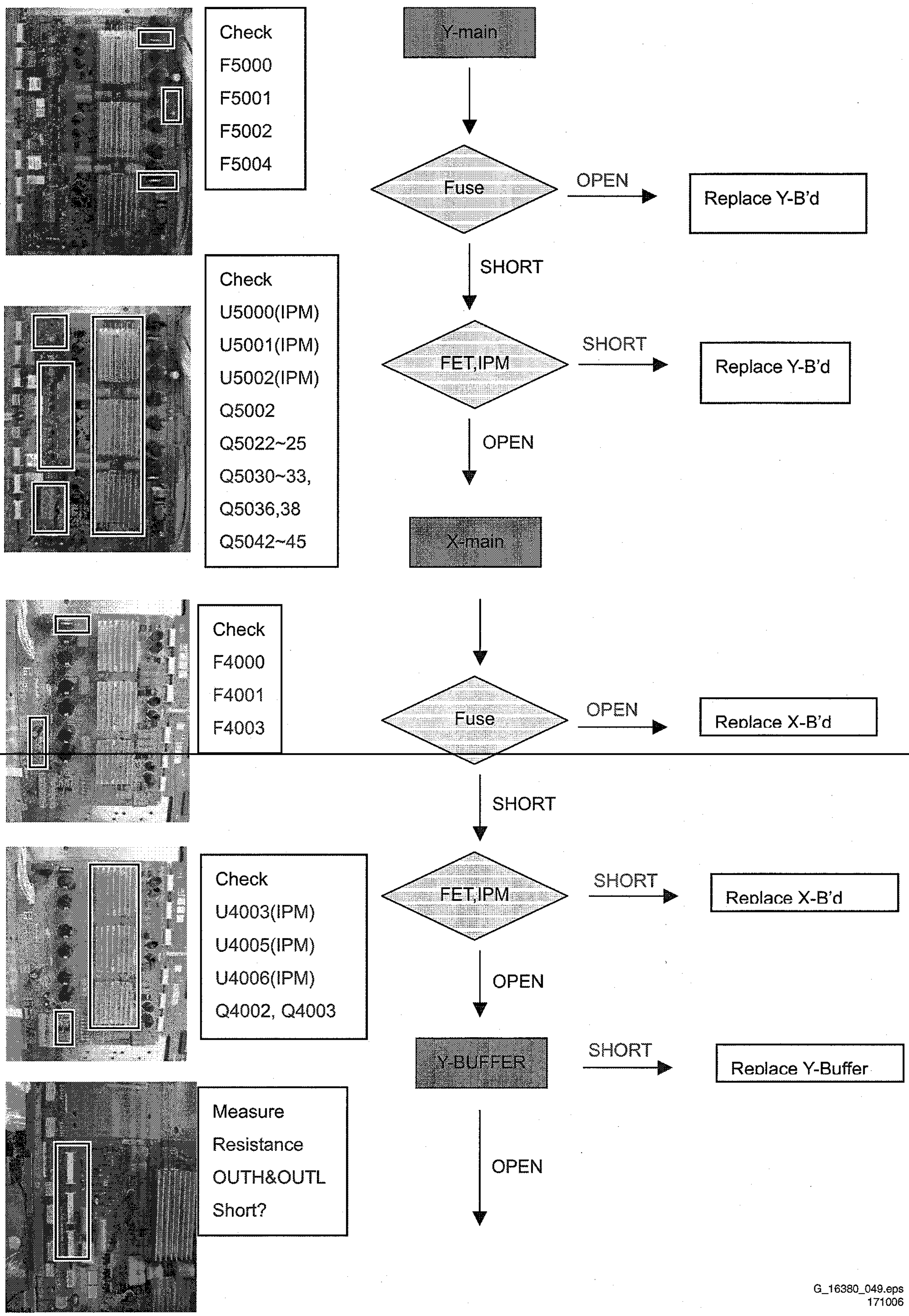
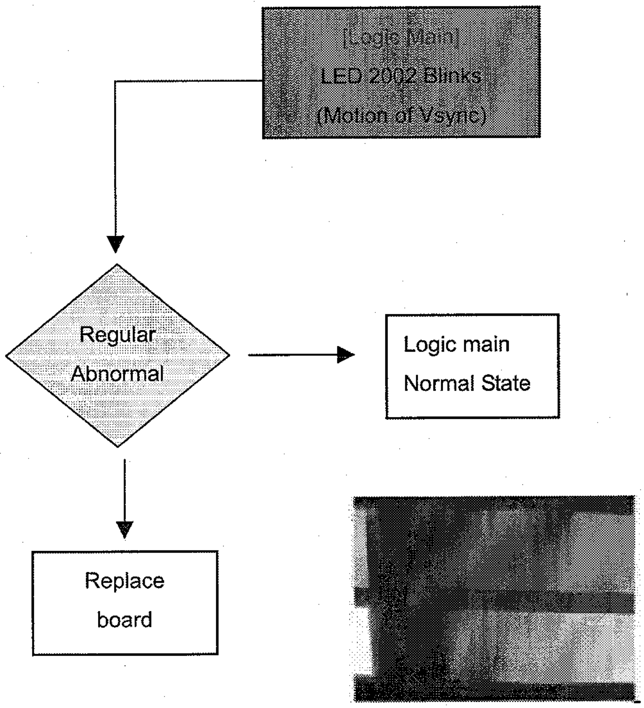

Check
F5000
F5001
F5002
F5004
Y-main
Fuse
OPEN
Replace Y-B'd
SHORT
Check
U5000(IPM)
U5001(IPM)
U5002(IPM)
Q5002
Q5022~25
Q5030~33,
Q5036,38
Q5042~45
FET,IPM
SHORT
Replace Y-B'd
OPEN
X-main
Check
F4000
F4001
F4003
Fuse
OPEN
Replace X-B'd
SHORT
Check
U4003(IPM)
U4005(IPM)
U4006(IPM)
Q4002, Q4003
FET,IPM
SHORT
Replace X-B'd
OPEN
Y-BUFFER
SHORT
Replace Y-Buffer
Measure
Resistance
OUTH&OUTL
Short?
OPEN
G_16380_049.eps
171006

Figure 5-41 Fault symptom: "Abnormal Display" 63" HD v4 1/2

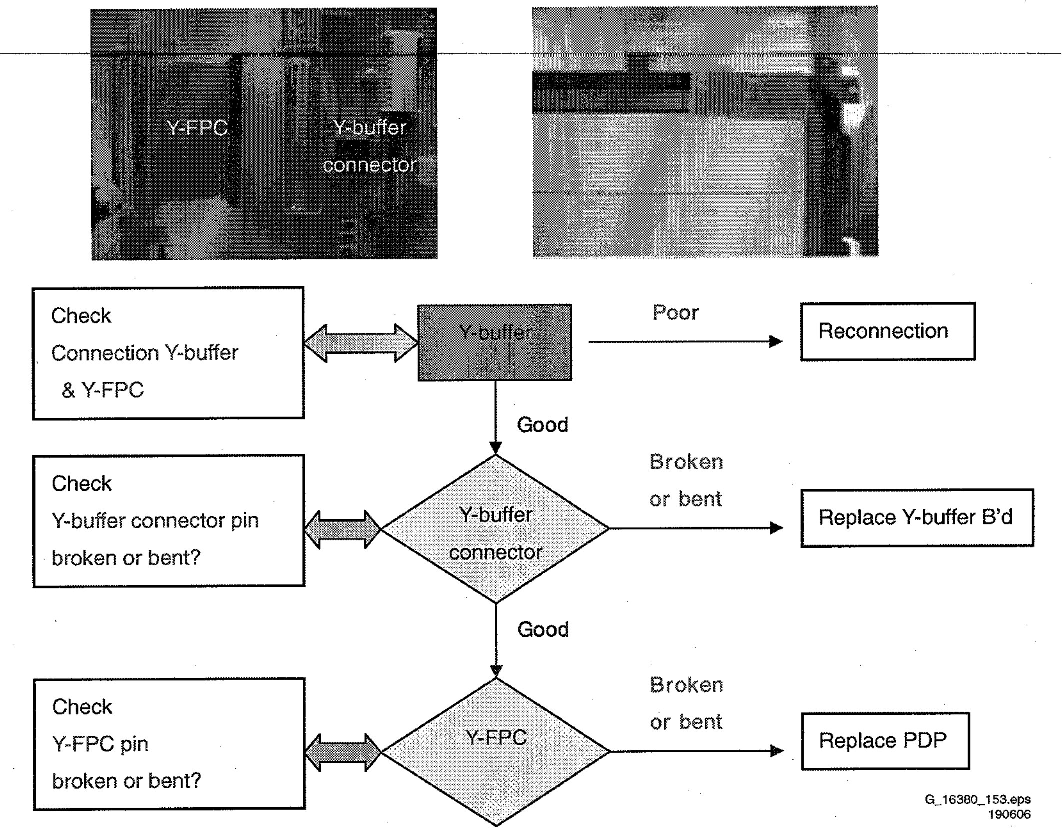

[Logic Main]
LED 2002 Blinks
(Motion of Vsync)
Regular
Abnormal
Logic main
Normal State
Replace
board

G_16380_050.eps
171006

Figure 5-42 Fault symptom: "Abnormal Display" 63" HD v4 2/2

5.2.5 Horizontal line or block open

(some horizontal lines don't exist on screen)


Y-FPC
Y-buffer
connector
Check
Connection Y-buffer
& Y-FPC
Y-buffer
Poor
Reconnection
Good
Check
Y-buffer connector pin
broken or bent?
Y-buffer
connector
Broken
or bent
Replace Y-buffer B'd
Good
Check
Y-FPC pin
broken or bent?
Y-FPC
Broken
or bent
Replace PDP

G_16380_153.eps
190606

Figure 5-43 Fault symptom: "Horizontal line or block open"

5.2.6 Address open

(some vertical lines don't exist on screen)

-> Address Open is related with Logic Main, Logic Buffer, FFC, TCP and so on.
This page shows you how to check the boards, and the following pages show you how to find the defective board.

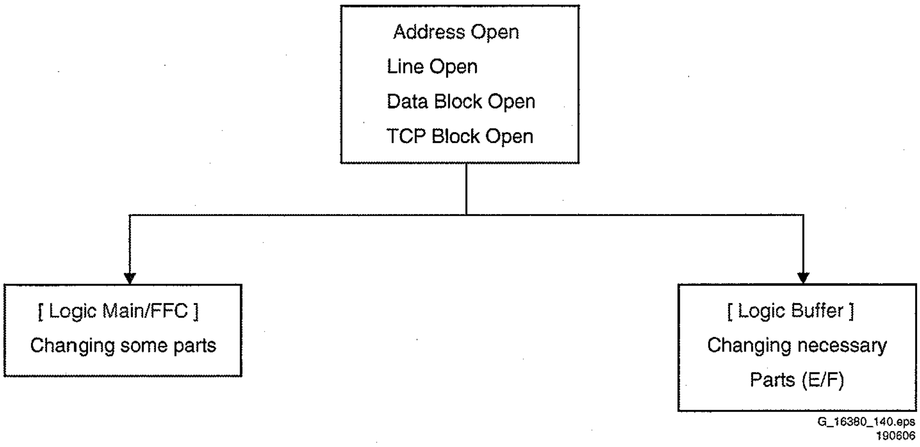

Address Open
Line Open
Data Block Open
TCP Block Open
[Logic Main/FFC]
Changing some parts
[Logic Buffer]
Changing necessary
Parts (E/F)
G_16380_140.eps
190606

Figure 5-44 Fault symptom: "Address open" 1/2

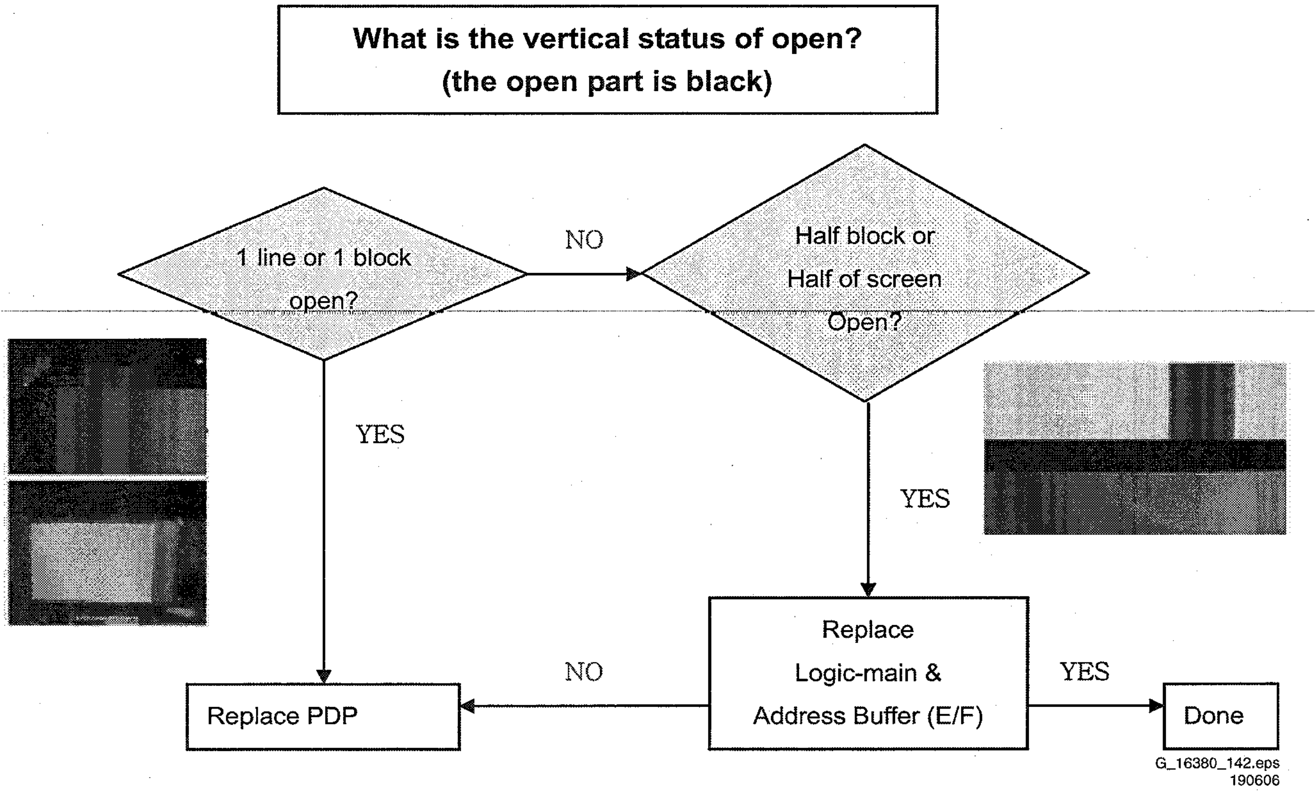

What is the vertical status of open?
(the open part is black)
1 line or 1 block open?
NO
Half block or Half of screen Open?
YES
YES
Replace Logic-main & Address Buffer (E/F)
NO
YES
Replace PDP
Done
G_16380_142.eps
190606

Figure 5-45 Fault symptom: "Address open" 2/2

5.2.7 Address short

(some vertical lines appear to be linked on screen)

-> Address Short is related with Logic Main, Logic Buffer, FFC, TCP and so on.
This page shows you how to check the boards, and the following pages show you how to find the defective board.

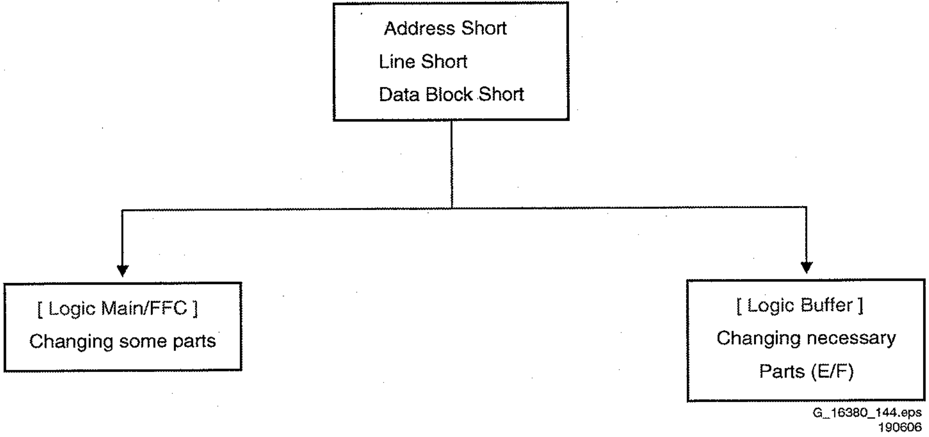

Address Short
Line Short
Data Block Short
[Logic Main/FFC]
Changing some parts
[Logic Buffer]
Changing necessary
Parts (E/F)
G_16380_144.eps
190606

Figure 5-46 Fault symptom: "Address short" 1/2

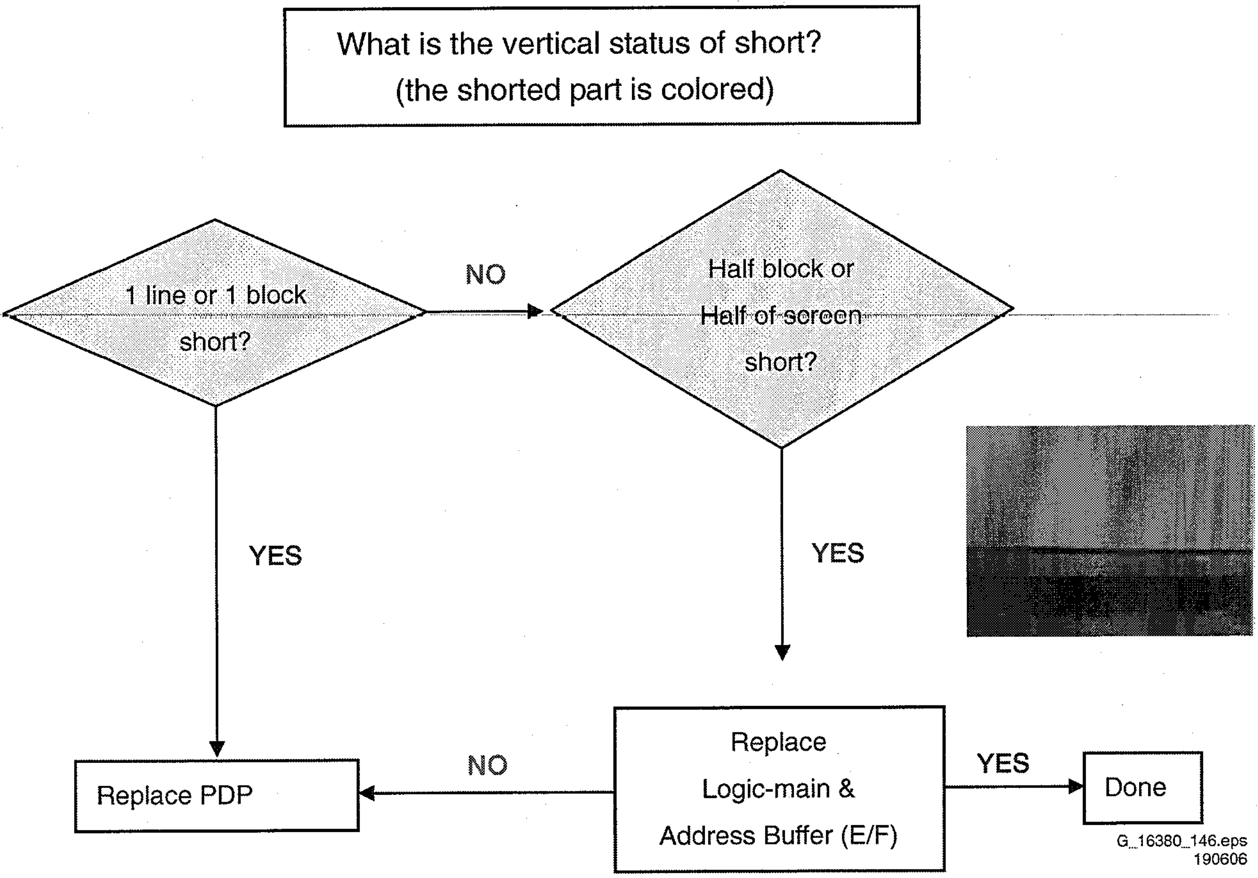
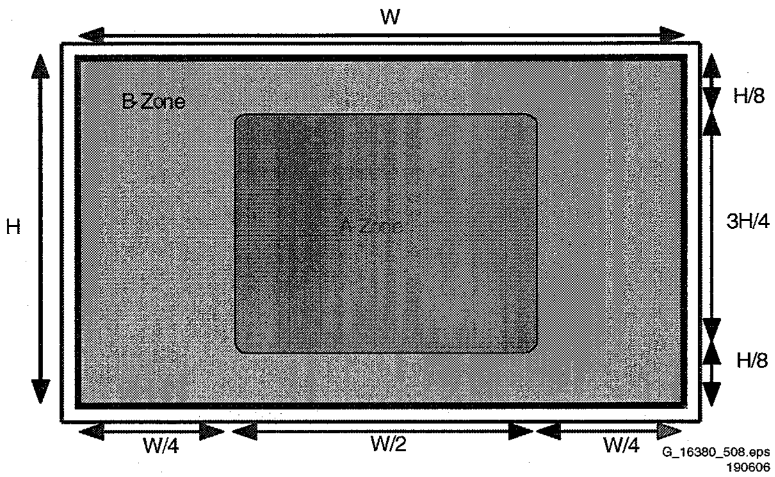

What is the vertical status of short?
(the shorted part is colored)
1 line or 1 block
short?
NO
Half block or
Half of screen
short?
YES
YES
Replace PDP
NO
Replace
Logic-main &
Address Buffer (E/F)
YES
Done
G_16380_146.eps
190606

Figure 5-47 Fault symptom: "Address short" 2/2

5.2.8 Criteria for Panel Replacement, due to Defective Panel Cells



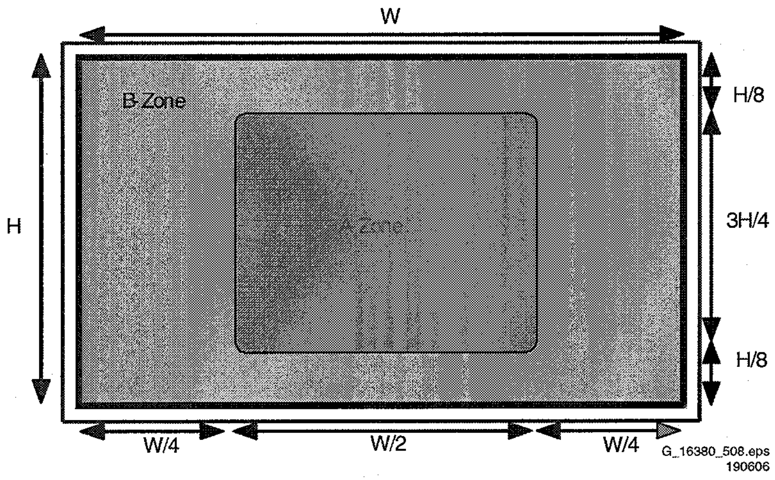
G_16380_508.eps
190606

Figure 5-48 Panel zones 42” SD v5

Item	Specification	
	Number of cell defects	Distance between cell defects
Non-lighting cell defect	Zone A: 0 and less Zone B: 4 and less	Regardless of A and B zone 1 Cell Defect in an area of 50 * 50 mm
Non-extinguishing cell defect	Zone A: 0 Zone B: 1	
Flickering cell defect	Zone A: 0 Zone B: 1	
High Intensity Cell defect	Zone A: 0 Zone B: 0	
Adjacent cell defect	Zone A: 0 Zone B: 0	
Total cell defects	6 and less	

G_16380_509.eps
190606

Figure 5-49 Criteria for panel replacement 42” SD v5



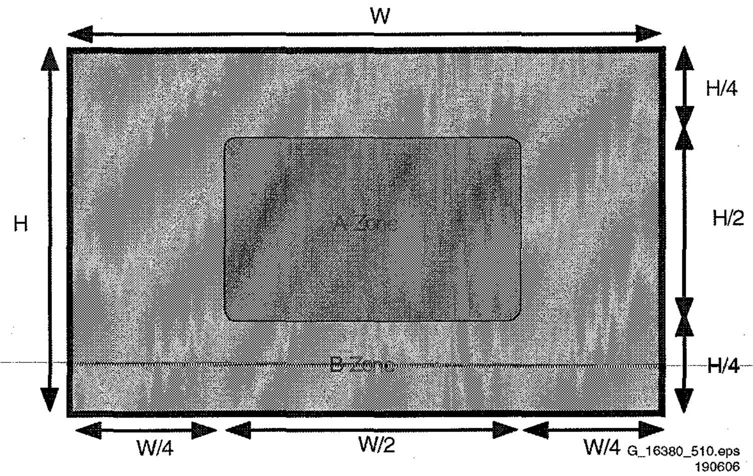
G_16380_508.eps
190606

Figure 5-50 Panel zones 42” HD w1

Item	Specification	
	Number of cell defects	Distance between cell defects
Non-lighting cell defect	Zone A: 4 and less Zone B: 8 and less	Regardless of A and B zone, 1 Cell Defect in an area of 50mm*50mm
Non-extinguishing cell defect	Zone A: 0 Zone B: 1 and less	
Flickering cell defect	Zone A: 0 Zone B: 1 and less	
High Intensity Cell defect	Zone A: 0 Zone B: 1 and less (Only Red & Blue)	
Adjacent cell defect	Zone A: 0 Zone B: 1 and less (Only Red & Blue)	
Total cell defects	12 and less	

G_16380_511.eps
190606

Figure 5-51 Criteria for panel replacement 42" HD w1



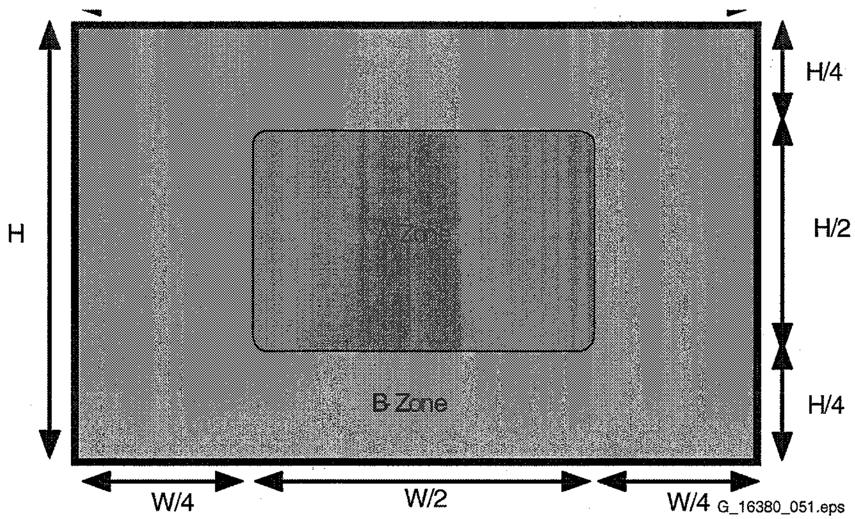
G_16380_510.eps
190606

Figure 5-52 Panel zones 50" HD w1

Item	Specification	
	Number of cell defects	Distance between cell defects
Non-lighting cell defect	Zone A: 4 and less Zone B: 8 and less	Regardless of A and B zone, 1 Cell Defect in an area of 50mm*50mm
Non-extinguishing cell defect	Zone A: 0 Zone B: 1 and less	
Flickering cell defect	Zone A: 0 Zone B: 1 and less	
High Intensity Cell defect	Zone A: 0 Zone B: 1 and less (Only Red & Blue)	
Adjacent cell defect	Zone A: 0 Zone B: 1 and less (Only Red & Blue)	
Total cell defects	12 and less	

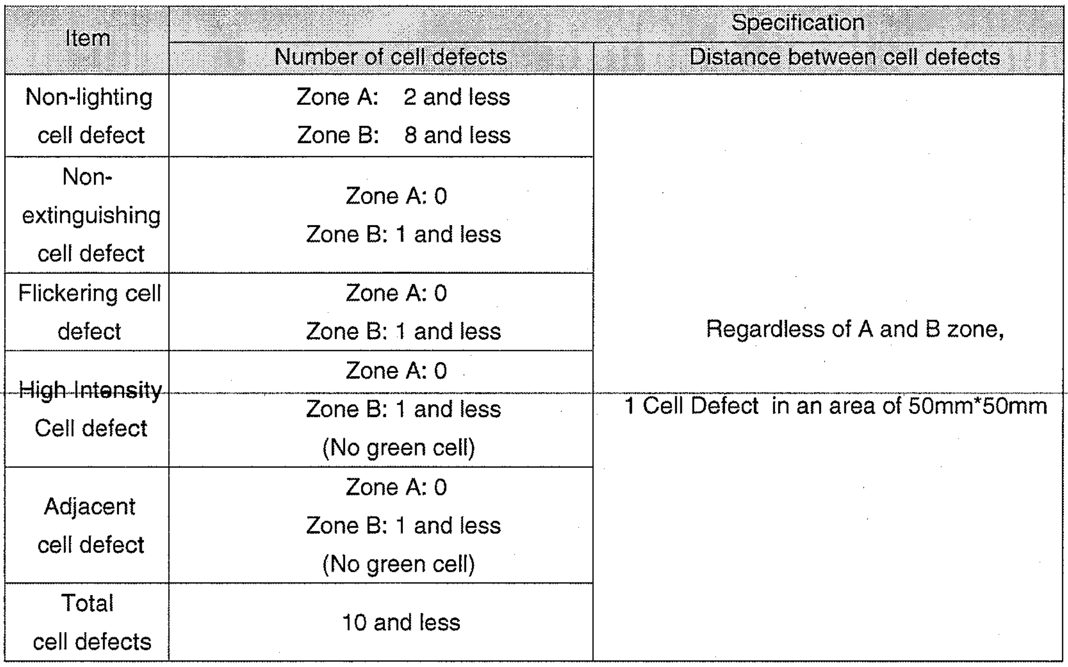
G_16380_511.eps
190606

Figure 5-53 Criteria for panel replacement 50" HD w1



G_16380_051.eps
171006

Figure 5-54 Panel zones 63" HD v4



Item	Specification	
	Number of cell defects	Distance between cell defects
Non-lighting cell defect	Zone A: 2 and less Zone B: 8 and less	Regardless of A and B zone, 1 Cell Defect in an area of 50mm*50mm
Non-extinguishing cell defect	Zone A: 0 Zone B: 1 and less	
Flickering cell defect	Zone A: 0 Zone B: 1 and less	
High Intensity Cell defect	Zone A: 0 Zone B: 1 and less (No green cell)	
Adjacent cell defect	Zone A: 0 Zone B: 1 and less (No green cell)	
Total cell defects	10 and less	

G_16380_052.eps
171006

Figure 5-55 Criteria for panel replacement 63" HD v4

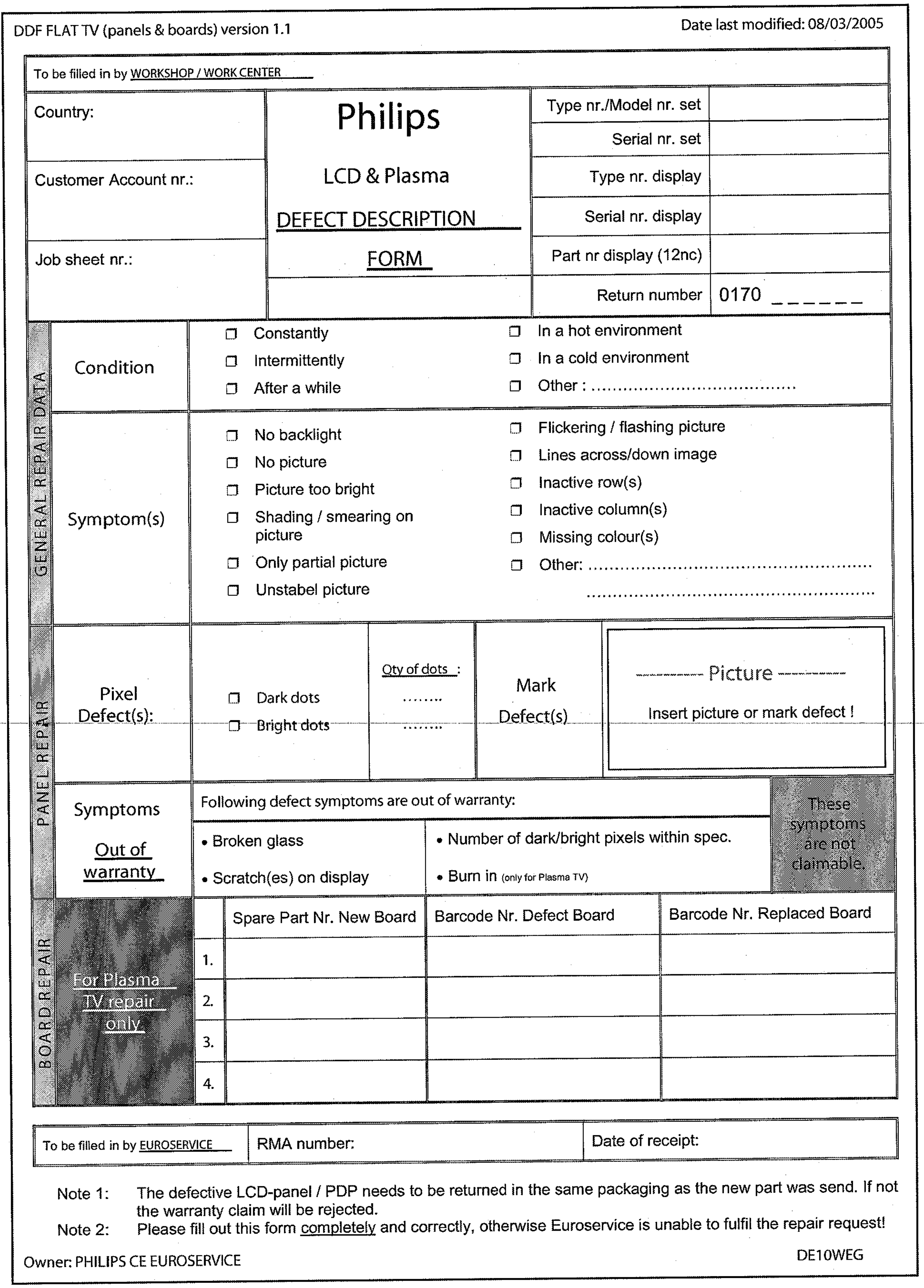
5.2.9 Overview

Table 5-2 Overview of faults and cures

Condition Name	Description	Related Board
No output voltage	Operating voltages don't exist.	SMPS
No display	Operating voltages exist, but no image on screen	Y-MAIN, X-MAIN, Logic Main, Cables
Abnormal display	Abnormal Image (not open or short) is on screen.	Y-MAIN, X-MAIN, Logic Main
Sustain open	Some horizontal lines are missing on screen	Scan Buffer, FPC of X / Y
Sustain short	Some horizontal lines appear to be linked on screen	Scan Buffer, FPC of X / Y
Address open	Some vertical lines are missing on screen	Logic Main, Logic Buffer, FFC,TCP
Address short	Some vertical lines appear to be linked on screen	Logic Main, Logic Buffer, FFC,TCP
Defective panel cells	Some cells seem to be defective	Check criteria for replacement of the panel

5.3 Defect Description Form

This form must be used by the workshops for warranty claims:



DDF FLAT TV (panels & boards) version 1.1

Date last modified: 08/03/2005

To be filled in by WORKSHOP / WORK CENTER

Country:	Philips	Type nr./Model nr. set	
		Serial nr. set	
Customer Account nr.:	LCD & Plasma	Type nr. display	
	DEFECT DESCRIPTION	Serial nr. display	
Job sheet nr.:	FORM	Part nr display (12nc)	
		Return number	0170 ______

GENERAL REPAIR DATA	Condition	☐ Constantly ☐ Intermittently ☐ After a while	☐ In a hot environment ☐ In a cold environment ☐ Other : ....
	Symptom(s)	☐ No backlight ☐ No picture ☐ Picture too bright ☐ Shading / smearing on picture ☐ Only partial picture ☐ Unstabel picture	☐ Flickering / flashing picture ☐ Lines across/down image ☐ Inactive row(s) ☐ Inactive column(s) ☐ Missing colour(s) ☐ Other: ....

PANEL REPAIR	Pixel Defect(s):	☐ Dark dots ☐ Bright dots	Qty of dots :	Mark Defect(s)	———— Picture ———— Insert picture or mark defect !

PANEL REPAIR	Symptoms Out of warranty	Following defect symptoms are out of warranty:		These symptoms are not claimable.
		• Broken glass • Scratch(es) on display	• Number of dark/bright pixels within spec. • Burn in (only for Plasma TV)	

BOARD REPAIR For Plasma TV repair only		Spare Part Nr. New Board	Barcode Nr. Defect Board	Barcode Nr. Replaced Board
	1.			
	2.			
	3.			
	4.			

To be filled in by EUROSERVICE	RMA number:	Date of receipt:

Note 1: The defective LCD-panel / PDP needs to be returned in the same packaging as the new part was send. If not the warranty claim will be rejected.

Note 2: Please fill out this form completely and correctly, otherwise Euroservice is unable to fulfil the repair request!

Owner: PHILIPS CE EUROSERVICE

DE10WEG

F_15590_115.eps
110705

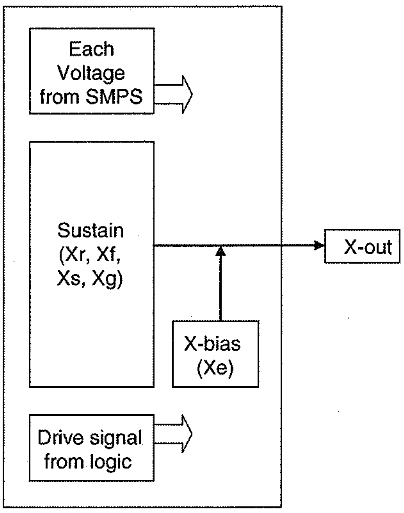
Figure 5-56 Defect Description Form (DDF)

6. Block Diagrams, Test Point Overview, and Waveforms

Index of this chapter:

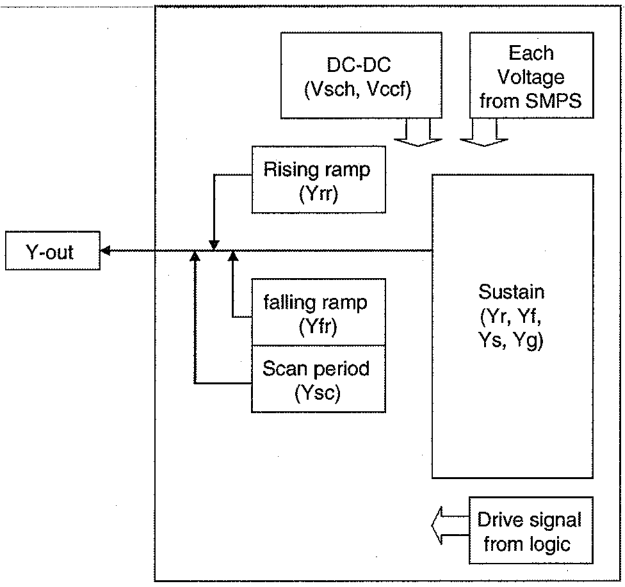
6.1 Block Diagram for Drive Circuits
6.2 Block Diagram for Logic Circuit
6.3 PSU
6.3.1 PSU Layout, Display Types 42" SD v5, 42" HD w1, and 50" HD w1
6.3.2 PSU Layout, Display Type 63" HD v4
6.3.3 Voltage Level Overview 42" SD v5
6.3.4 Voltage Level Overview 42" HD w1
6.3.5 Voltage Level Overview 50" HD w1
6.3.6 Voltage Level Overview 63" HD v4

6.1 Block Diagram for Drive Circuits


Each Voltage from SMPS
Sustain (Xr, Xf, Xs, Xg)
X-out
X-bias (Xe)
Drive signal from logic

G_16380_218.eps
190606

Figure 6-1 Block diagram X-Main Board


DC-DC (Vsch, Vccf)
Each Voltage from SMPS
Rising ramp (Yrr)
Y-out
falling ramp (Yfr)
Scan period (Ysc)
Sustain (Yr, Yf, Ys, Yg)
Drive signal from logic

G_16380_219.eps
190606

Figure 6-2 Block diagram Y-Main Board

6.2 Block Diagram for Logic Circuit

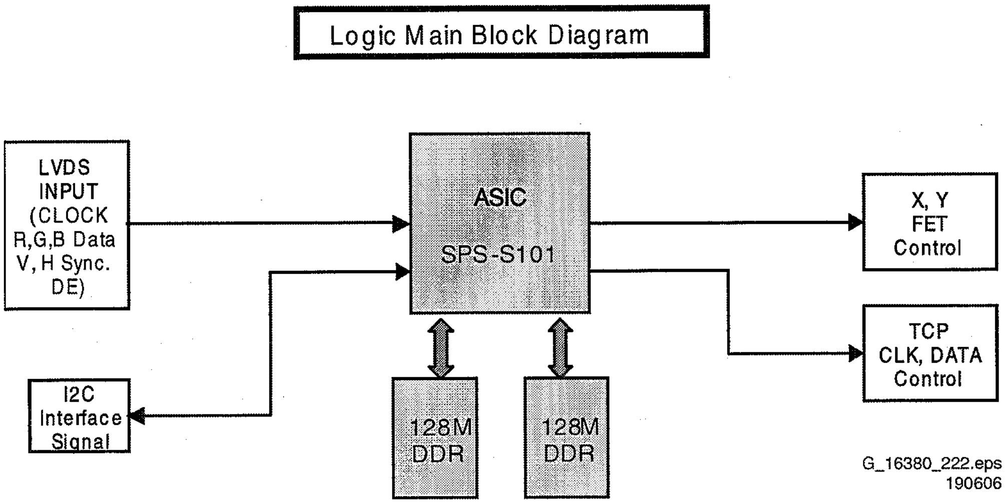

Logic Main Block Diagram
LVDS INPUT (CLOCK R,G,B Data V, H Sync. DE)
I2C Interface Signal
ASIC
SPS-S101
128M DDR
128M DDR
X, Y FET Control
TCP CLK, DATA Control
G_16380_222.eps
190606

Figure 6-3 Block diagram (42" SD v5)

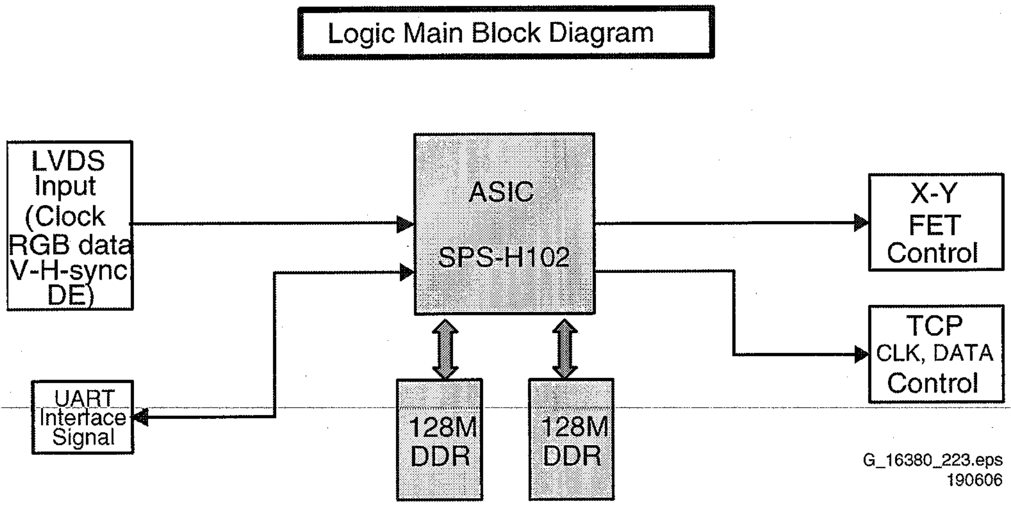

Logic Main Block Diagram
LVDS Input (Clock RGB data V-H-sync DE)
UART Interface Signal
ASIC
SPS-H102
128M DDR
128M DDR
X-Y FET Control
TCP CLK, DATA Control
G_16380_223.eps
190606

Figure 6-4 Block diagram (42" HD w1)

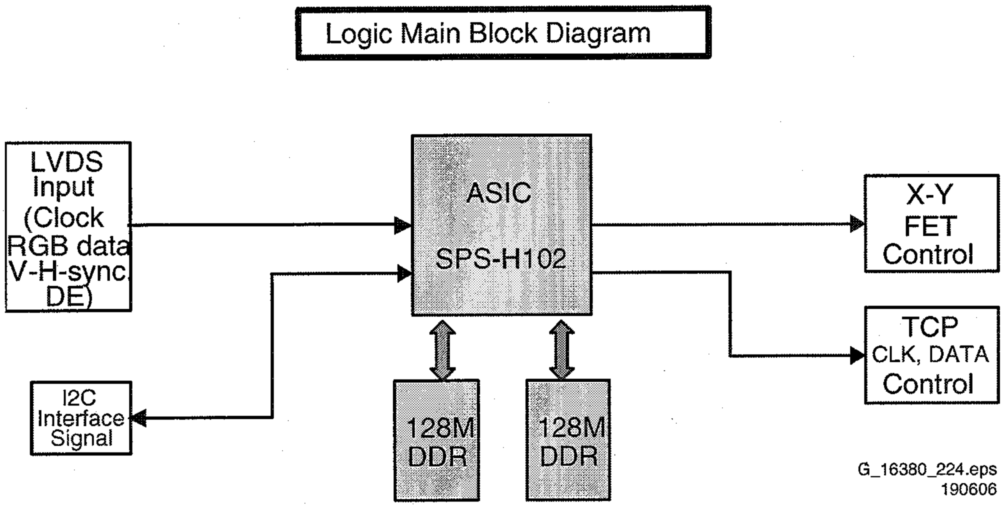
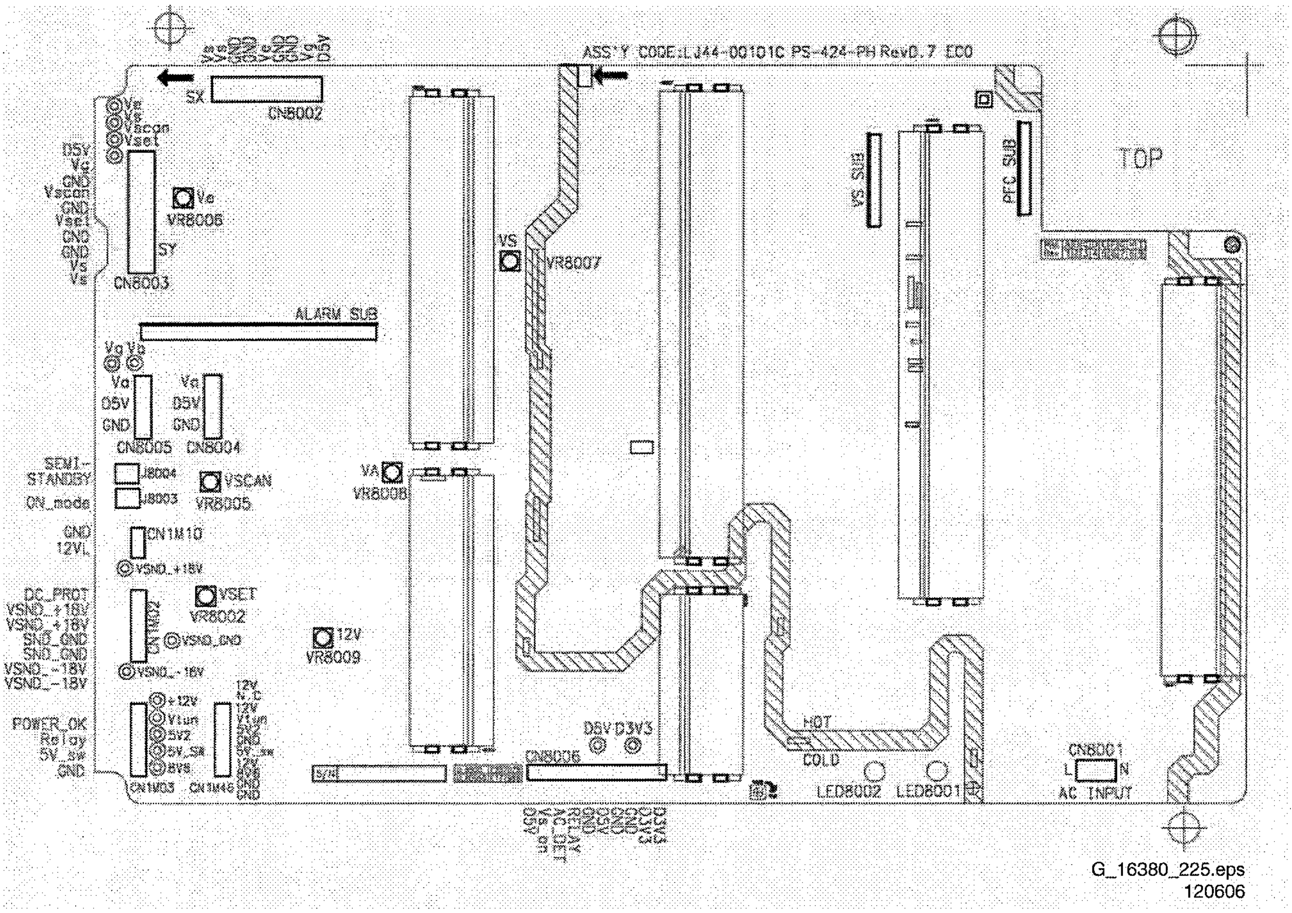

Logic Main Block Diagram
LVDS Input (Clock RGB data V-H-sync DE)
I2C Interface Signal
ASIC
SPS-H102
128M DDR
128M DDR
X-Y FET Control
TCP CLK, DATA Control
G_16380_224.eps
190606

Figure 6-5 Block diagram (50" HD w1 and 63” HD v4)

6.3 PSU

6.3.1 PSU Layout, Display Types 42" SD v5, 42" HD w1, and 50" HD w1

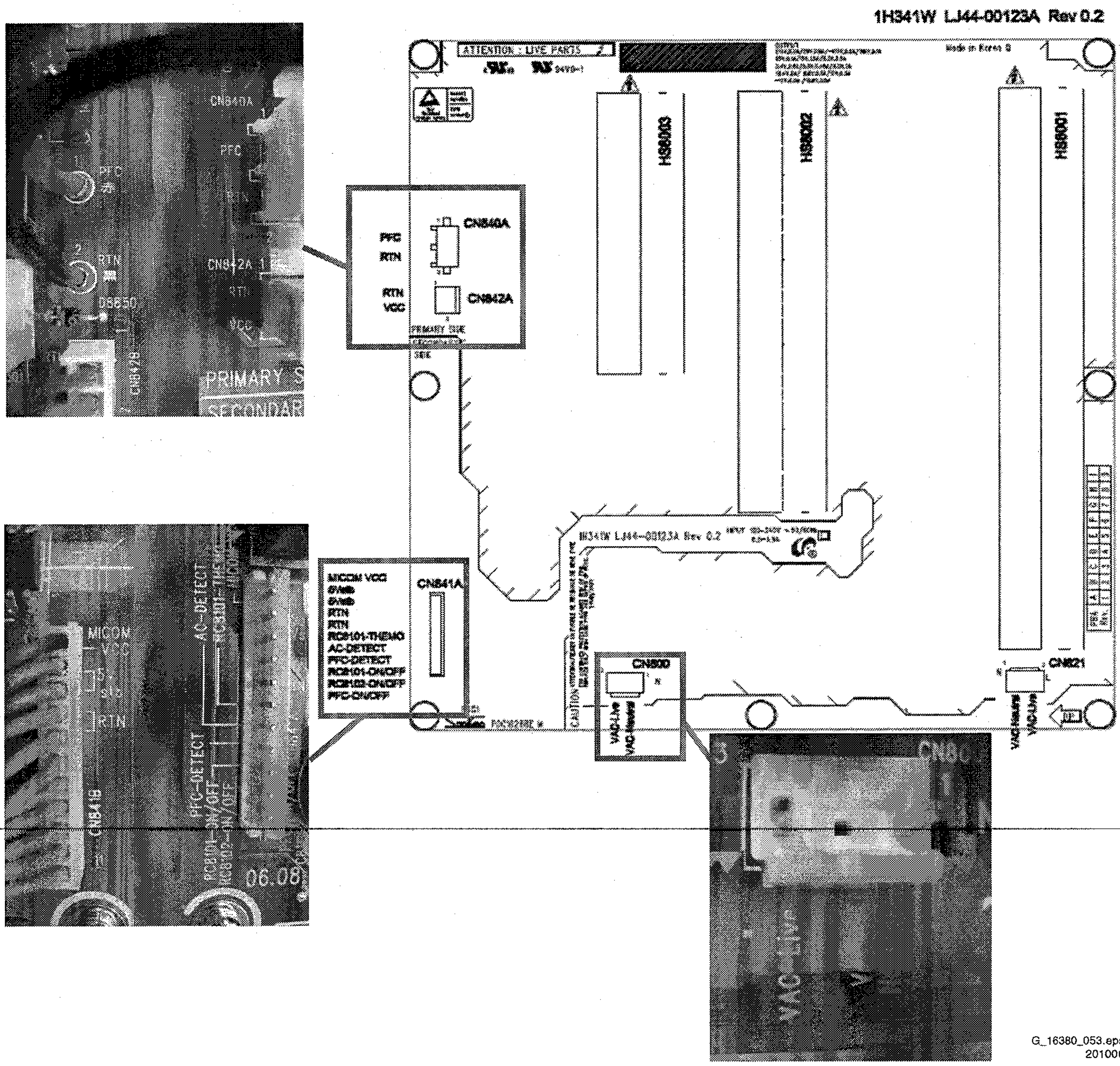

ASS'Y CODE:LJ44-00101C PS-424-PH Rev0.7 ECO
Vs Vs GND GND Ve GND GND Vg D5V
SX
CN8002
Ve
Vs
Vscan
Vset
D5V
Vg
GND
Vscan
GND
Vset
GND
GND
Vs
Vs
Ve
VR8006
SY
CN8003
VS
VR8007
ALARM SUB
Va Va
Va D5V GND
Va D5V GND
CN8005 CN8004
SEMI-STANDBY
ON_mode
J8004
J8003
VSCAN
VR8005
VA
VR8008
GND
12VL
CN1M10
VSND_+18V
DC_PROT
VSND_+18V
VSND_+18V
SND_GND
SND_GND
VSND_-18V
VSND_-18V
VSET
VR8002
VSND_GND
VSND_-18V
12V
VR8009
POWER_OK
Relay
5V_sw
GND
+12V
V1un
5V2
5V_SW
8VS
CN1M03 CN1M46
12V
N.C
12V
V1un
5V2
GND
5V_sw
12V
GND
GND
GND
S/N
CN8006
D5V D3V3
D5V_on Vs_on AC_DET RELAY GND D5V GND GND D3V3 D3V3
HOT
COLD
LED8002 LED8001
CN8001
L N
AC INPUT
VS SUB
PFC SUB
TOP

G_16380_225.eps
120606

Figure 6-6 PSU layout (42" SD v5, 42" HD w1, and 50" HD w1)

6.3.2 PSU Layout, Display Type 63" HD v4

Package 1, Main Supply


1H341W LJ44-00123A Rev 0.2
ATTENTION : LIVE PARTS
HS8003
HS8002
HS8001
CN840A
PFC
RTN
RTN
VCC
CN842A
PRIMARY SIDE
MICOM VCC
5Vstb
5Vstb
RTN
RTN
RC8101-THEMO
AC-DETECT
PFC-DETECT
RC8101-ON/OFF
RC8102-ON/OFF
PFC-ON/OFF
CN841A
CN800
VAC-Live
VAC-Neutral
CN821
VAC-Neutral
VAC-Live
CN841B
CN842B
VAC-Live

G_16380_053.eps
201006

Figure 6-7 PSU layout (63" HD v4, Main PSU)

Package 2, Sub Supply

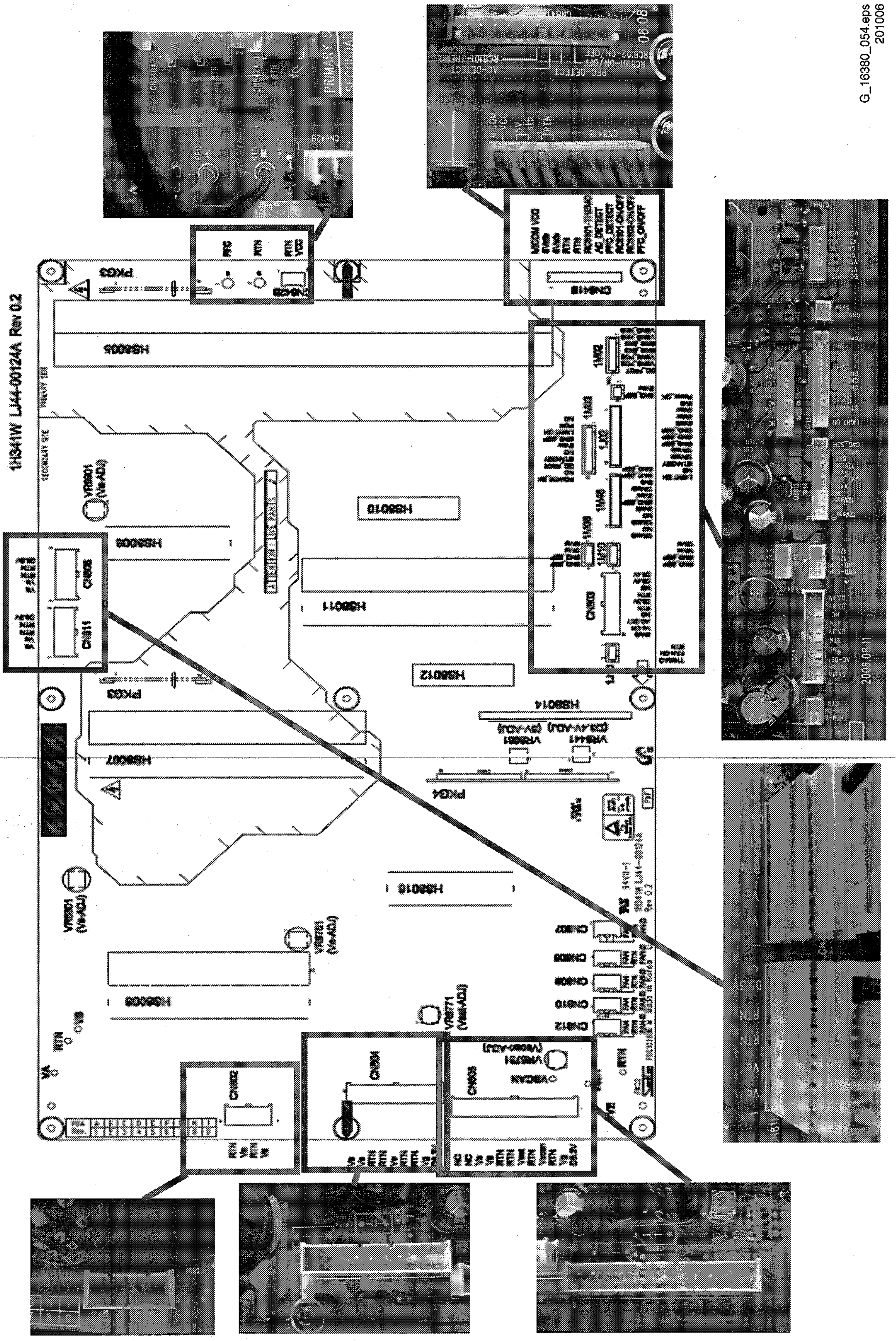

1H341W LJ44-00124A Rev 0.2
HS8005
HS8008
HS8010
HS8011
HS8012
HS8014
HS8007
HS8016
HS8009
CN8418
CN8428
CN8002
CN8004
CN8006
CN8803
PKG3
PKG4
VA
RTN
VR8801 (Va-ADJ)
VR8761 (Va-ADJ)
VR8771 (Vset-ADJ)
VR8751 (Vscan-ADJ)
VR8441 (D3.3V-ADJ)
VR8061 (5V-ADJ)
AC-DETECT
PFC-DETECT
PRIMARY SIDE
SECONDARY SIDE
2006.08.11

Figure 6-8 PSU layout (63" HD v4, Sub PSU))

G_16380_054.eps
201006

6.3.3 Voltage Level Overview 42" SD v5

Table 6-1 Voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	207 V ± 1 %	195 V ~ 215 V
2	VA	65 V ± 1.5 %	50 V ~ 70 V
3	VE	110 V ± 1.5 %	70 V ~ 110 V
4	VSET	201 V ± 1.5 %	180 V ~ 210 V
5	VSCAN	-190 V ± 1.5 %	-190 V ~ -170 V
6	VSB	5 V ± 5 %	Fixed
7	VG	15 V ± 5 %	Fixed
8	D5VL	5.2 V ± 5 %	Fixed
9	D3V3	3.3 V ± 5 %	Fixed
Check voltage label on the PDP for correct values.			

6.3.4 Voltage Level Overview 42" HD w1

Table 6-2 Voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	200 V ± 1.5 %	198 V ~ 202 V
2	VA	65 V ± 1.5 %	63 V ~ 67 V
3	VE	110 V ± 1.5 %	105 V ~ 115 V
4	VSET	195 V ± 1.5 %	193 V ~ 197 V
5	VSCAN	-190 V ± 1.5 %	-192 V ~ -188 V
6	VG	15 V ± 5 %	Fixed
7	D5VL	5.2 V ± 5 %	Fixed
8	D3V3	3.3 V ± 5 %	Fixed
Check voltage label on the PDP for correct values.			

6.3.5 Voltage Level Overview 50" HD w1

Table 6-3 Voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	202 V ± 1 %	190 V ~ 210 V
2	VA	65 V ± 1.5 %	55 V ~ 75 V
3	VE	115 V ± 1.5 %	110 V ~ 130 V
4	VSET	190 V ± 1.5 %	170 V ~ 200 V
5	VSCAN	-190 V ± 1.5 %	-210 V ~ -180 V
6	VSB	5 V ± 5 %	Fixed
7	VG	15 V ± 5 %	Fixed
8	D5VL	5.2 V ± 5 %	Fixed
9	D3V3	3.3 V ± 5 %	Fixed
Check voltage label on the PDP for correct values.			

6.3.6 Voltage Level Overview 63" HD v4

Table 6-4 Voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	184 V ± 1 %	165 V ~ 190 V
2	VA	72 V ± 1.5 %	60 V ~ 85 V
3	VE	88 V ± 1.5 %	80 V ~ 110 V
4	VSET	178 V ± 1.5 %	160 V ~ 200 V
5	VSCAN	-160 V ± 1.5 %	-190 V ~ -155 V
6	VSB	5 V ± 5 %	Fixed
7	VG	15 V ± 5 %	Fixed
8	D5VL	5.3 V ± 5 %	Fixed
9	D3V3	3.4 V ± 5 %	Fixed
Check voltage label on the PDP for correct values.			

7. Circuit Diagrams and PWB Layouts

Not applicable.

8. Alignments

Index of this chapter:

8.1 Power Supply Voltages
8.2 Waveform Alignments 42" SD v5
8.3 Waveform Alignments 42" HD w1
8.4 Waveform Alignments 50" HD w1
8.5 Waveform Alignments 63" HD v4

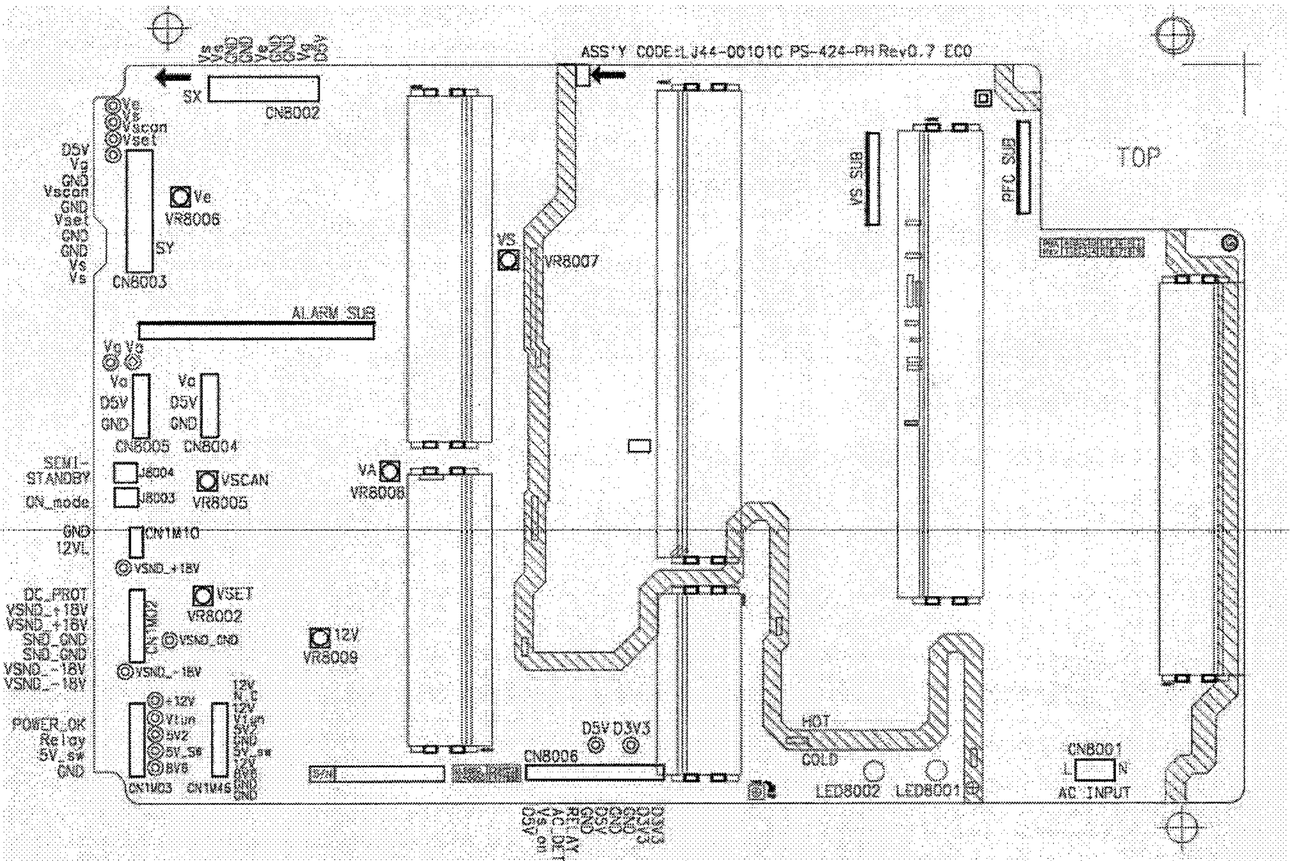
Note:

- Figures can deviate due to the different model executions.

Important: Remove all non-default jumpers and reset all DIP switches, after the repair!

8.1 Power Supply Voltages

8.1.1 Location of potentiometers and test points on the PSU of 42"SD v5, 42" HD w1, and 50" HD w1


ASS'Y CODE:LJ44-00101C PS-424-PH Rev0.7 ECO
SX
CN8002
Ve
Vs
Vscan
Vset
D5V
Va
GND
Vscan
GND
Vset
GND
GND
Vs
Vs
CN8003
SY
Ve
VR8006
Vs
VR8007
VS SUB
PFC SUB
TOP
ALARM SUB
Va Va
Va
D5V
GND
Va
D5V
GND
CN8005
CN8004
SEMI-STANDBY
ON_mode
J8004
J8003
VSCAN
VR8005
VA
VR8008
GND
12VL
CN1M10
VSND_+18V
DC_PROT
VSND_+18V
VSND_+18V
SND_GND
SND_GND
VSND_-18V
VSND_-18V
VSET
VR8002
VSND_GND
VSND_-18V
12V
VR8009
POWER_OK
Relay
5V_sw
GND
+12V
V1un
5V2
5V_SW
8V6
CN1M03
CN1M45
12V
N_C
12V
V1un
5V2
GND
5V_sw
12V
8V6
GND
GND
D5V D3V3
CN8006
HOT
COLD
LED8002
LED8001
CN8001
L
N
AC INPUT
D5V
Vs_on
AC_DET
RELAY
GND
D5V
D5V
GND
D3V3
D3V3

G_16380_225.eps
120606

Figure 8-1 Location of potentiometers and test points on the PSU of 42"SD v5, 42" HD w1, and 50" HD w1

8.1.2 Location of potentiometers and test points on the PSU of 63" HD v4

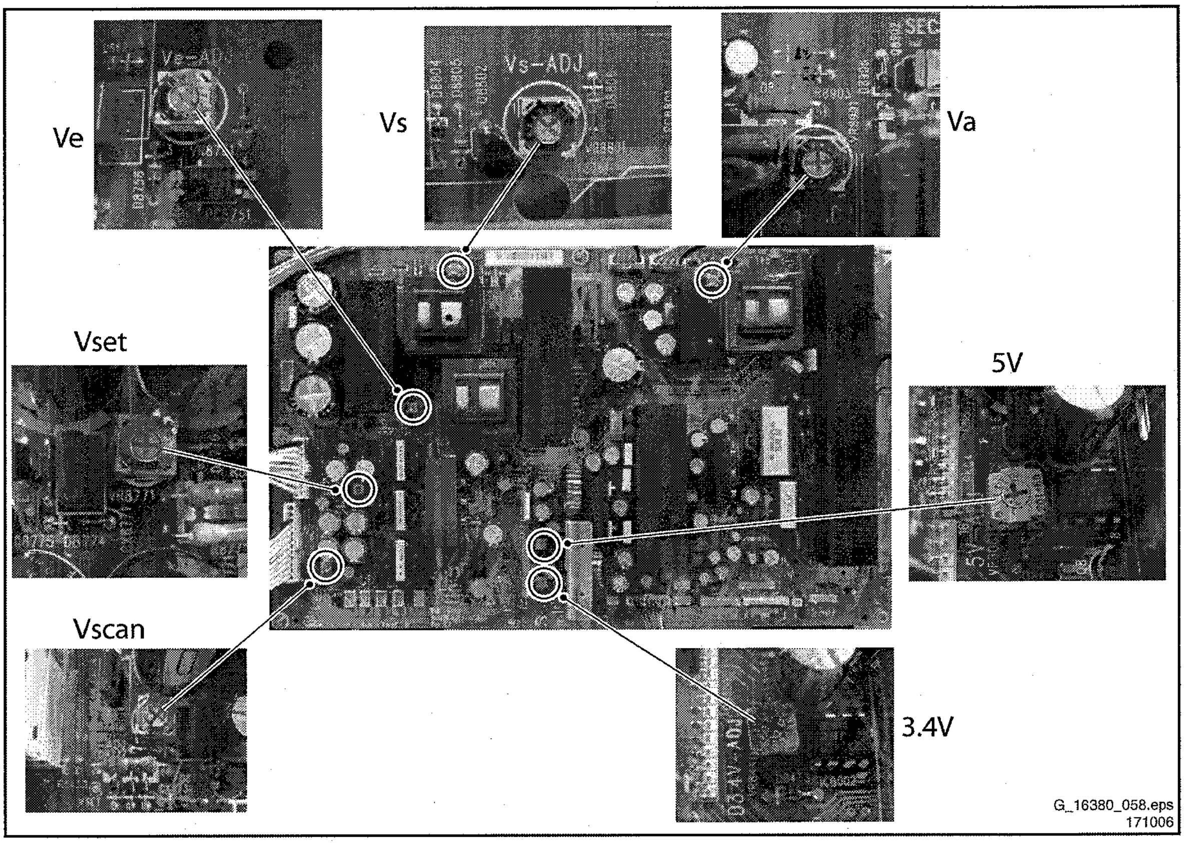

Ve
Vs
Va
Vset
5V
Vscan
3.4V
G_16380_058.eps
171006

Figure 8-2 Location of potentiometers on the PSU of 63" HD v4

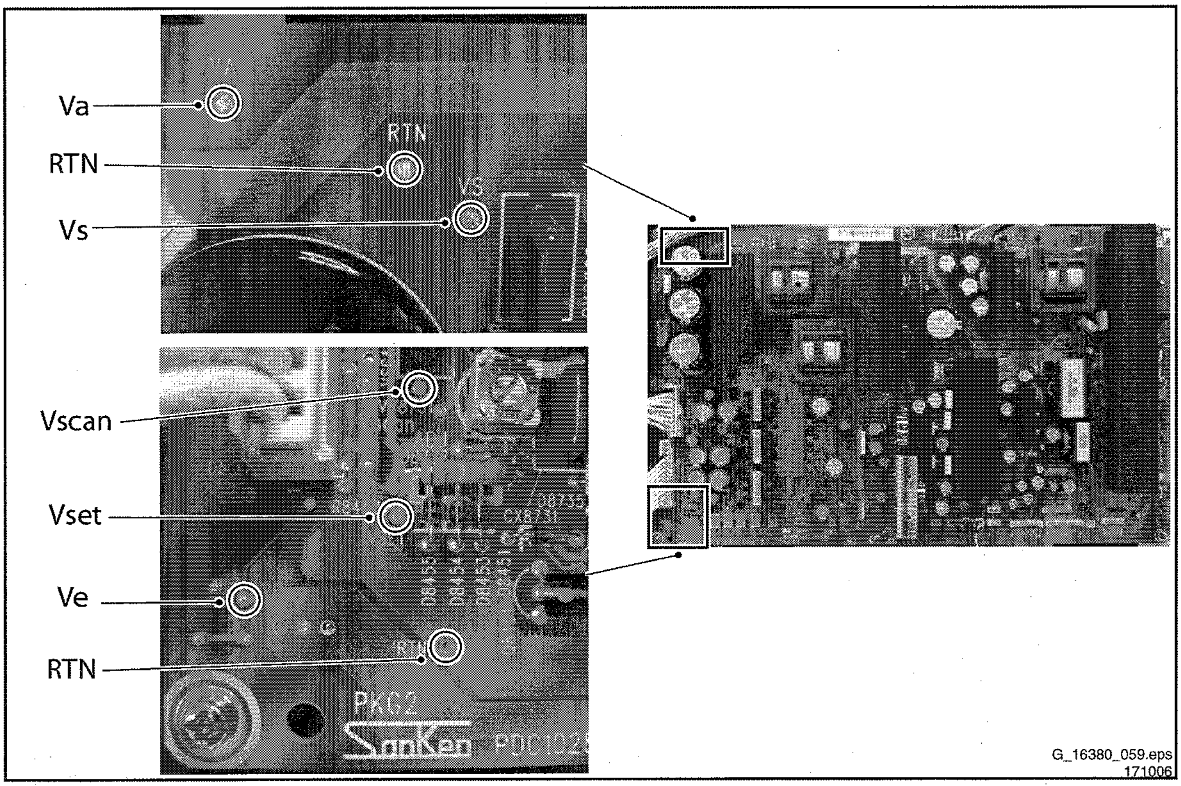
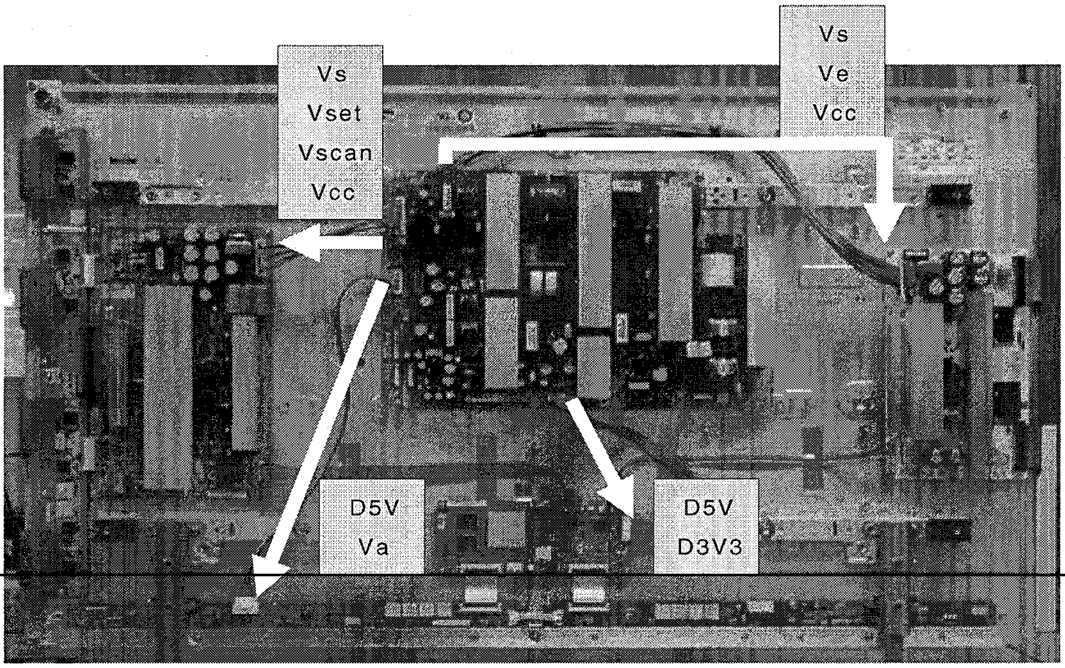

Va
RTN
Vs
Vscan
Vset
Ve
RTN
G_16380_059.eps
171006

Figure 8-3 Location of test points on the PSU of 63" HD v4

8.1.3 Adjustment Power Supply Voltages 42" SD v5

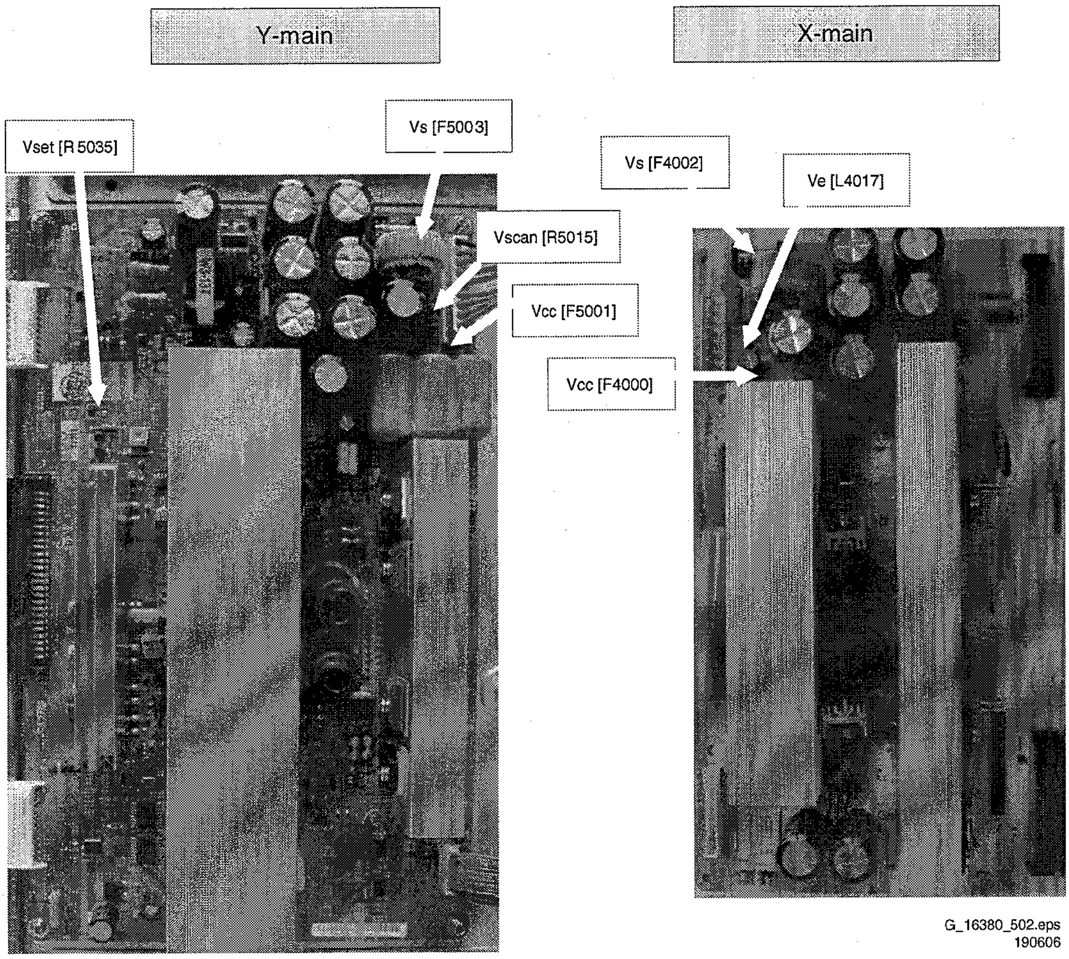
Table 8-1 Adjustment voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	207 V ± 1 %	195 V ~ 215 V
2	VA	65 V ± 1.5 %	50 V ~ 70 V
3	VE	110 V ± 1.5 %	70 V ~ 110 V
4	VSET	201 V ± 1.5 %	180 V ~ 210 V
5	VSCAN	-190 V ± 1.5 %	-190 V ~ -170 V
6	VSB	5 V ± 5 %	Fixed
7	VG	15 V ± 5 %	Fixed
8	D5VL	5.2 V ± 5 %	Fixed
9	D3V3	3.3 V ± 5 %	Fixed
Check voltage label on the PDP for correct values.			



G_16380_501.eps
190606

Figure 8-4 Location of the supply lines from the PSU to the boards - 42" SD v5


Y-main
X-main
Vset [R 5035]
Vs [F5003]
Vscan [R5015]
Vcc [F5001]
Vs [F4002]
Ve [L4017]
Vcc [F4000]

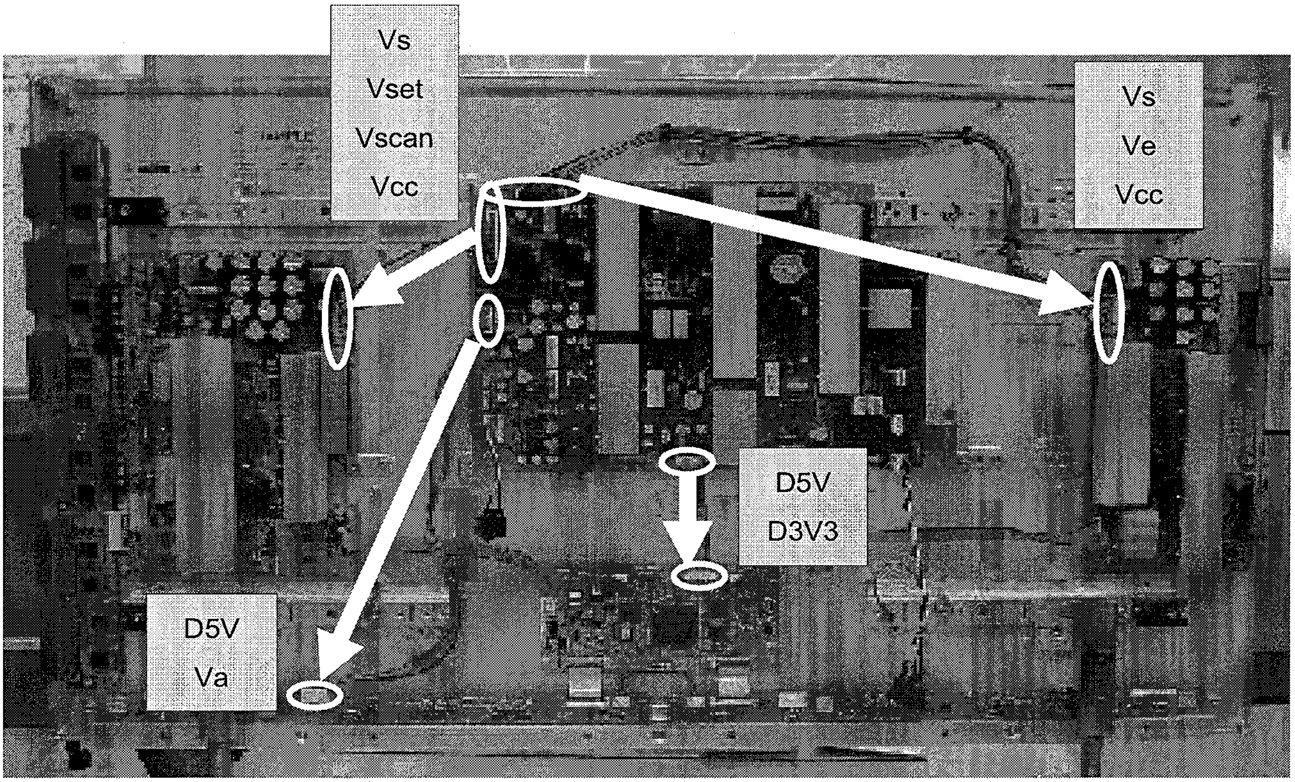
G_16380_502.eps
190606

Figure 8-5 Location of the test points for the supply voltages - 42" SD v5

8.1.4 Adjustment Power Supply Voltages 42" HD w1

Table 8-2 Adjustment voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	200 V ± 1.5 %	198 V ~ 202 V
2	VA	65 V ± 1.5 %	63 V ~ 67 V
3	VE	110 V ± 1.5 %	105 V ~ 115 V
4	VSET	195 V ± 1.5 %	193 V ~ 197 V
5	VSCAN	-190 V ± 1.5 %	-192 V ~ -188 V
6	VG	15 V ± 5 %	Fixed
7	D5VL	5.2 V ± 5 %	Fixed
8	D3V3	3.3 V ± 5 %	Fixed
Check voltage label on the PDP for correct values.			

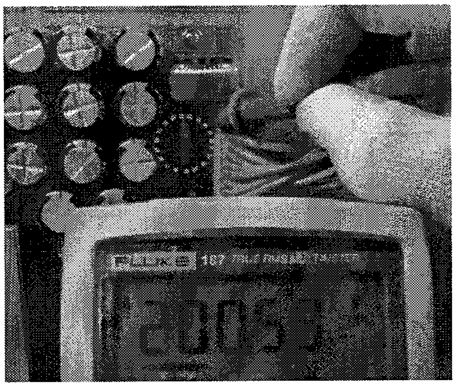

Vs
Vset
Vscan
Vcc
Vs
Ve
Vcc
D5V
D3V3
D5V
Va

G_16380_503.eps
160606

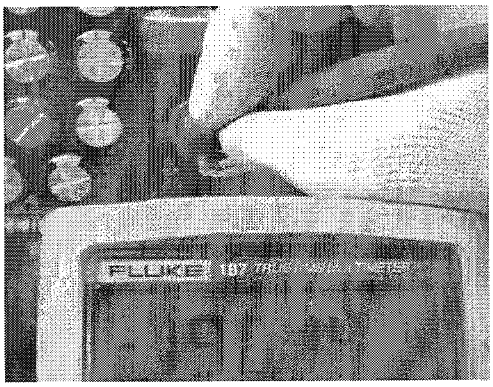
Figure 8-6 Location of the supply lines from the PSU to the boards - 42” HD w1

Drive board's voltage check point

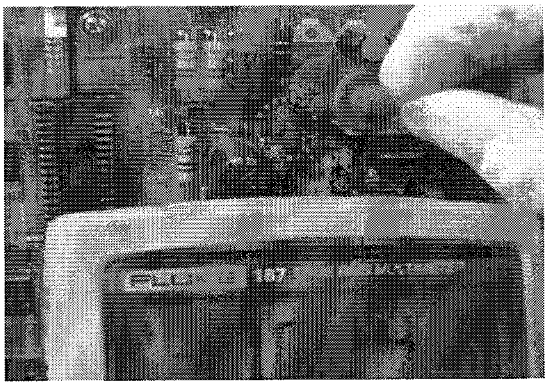
Y- main Voltage Check Point


FLUKE 187 TRUE RMS MULTIMETER

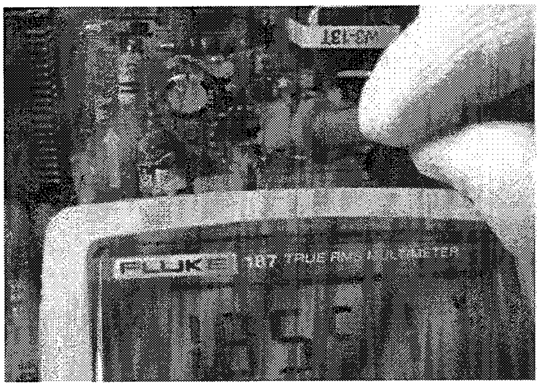
YM Vs (200V) – F5003


FLUKE 187 TRUE RMS MULTIMETER

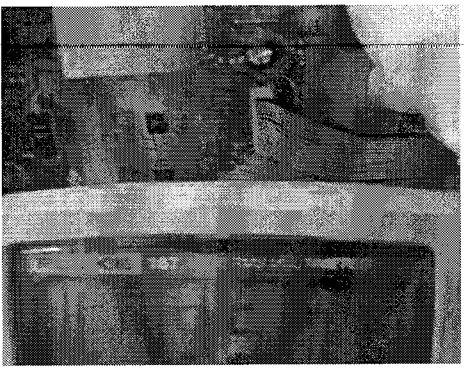
YM Vscan (-190V) – R5081



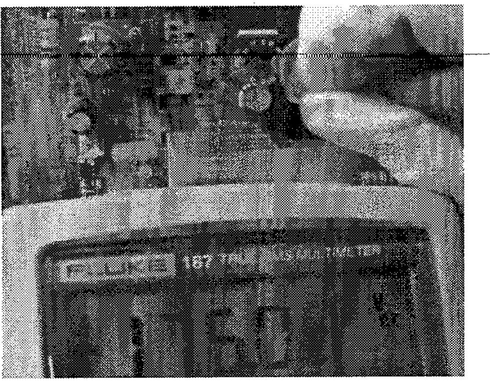
YM Vsch (-70V) – Vsch TP


FLUKE 187 TRUE RMS MULTIMETER

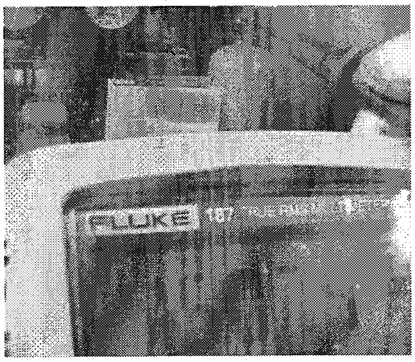
YM Vset (195V) – R5048



YM 5.5V (5.5V) – F5001


FLUKE 187 TRUE RMS MULTIMETER

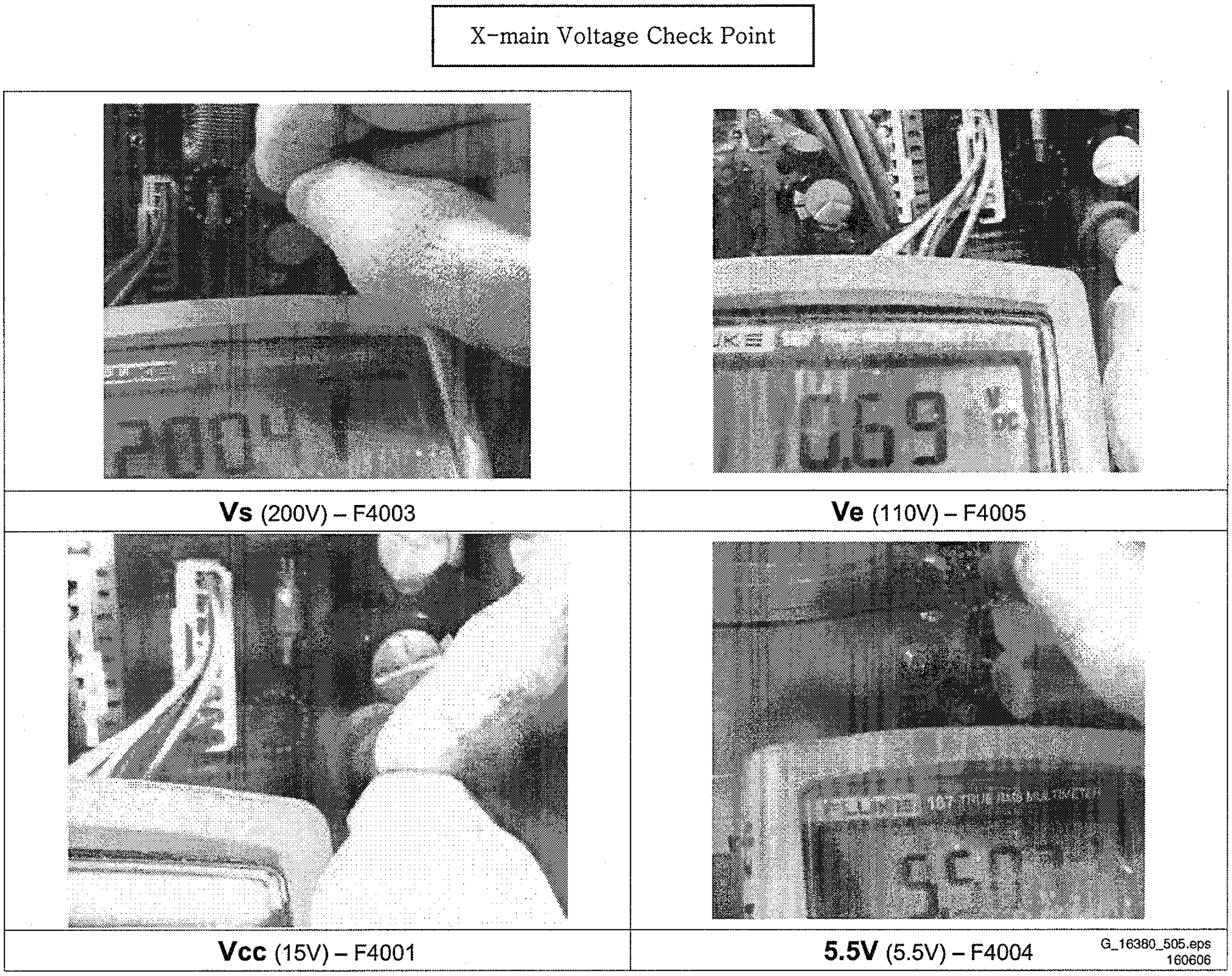
YM Vccf (Vscan + 15V) – Vccf TP



YM Vcc (15V) – F5004

G_16380_504.eps
160606

Figure 8-7 Location of the test points for the supply voltages - Y-main - 42" HD w1



Vs (200V) – F4003

Ve (110V) – F4005

Vcc (15V) – F4001

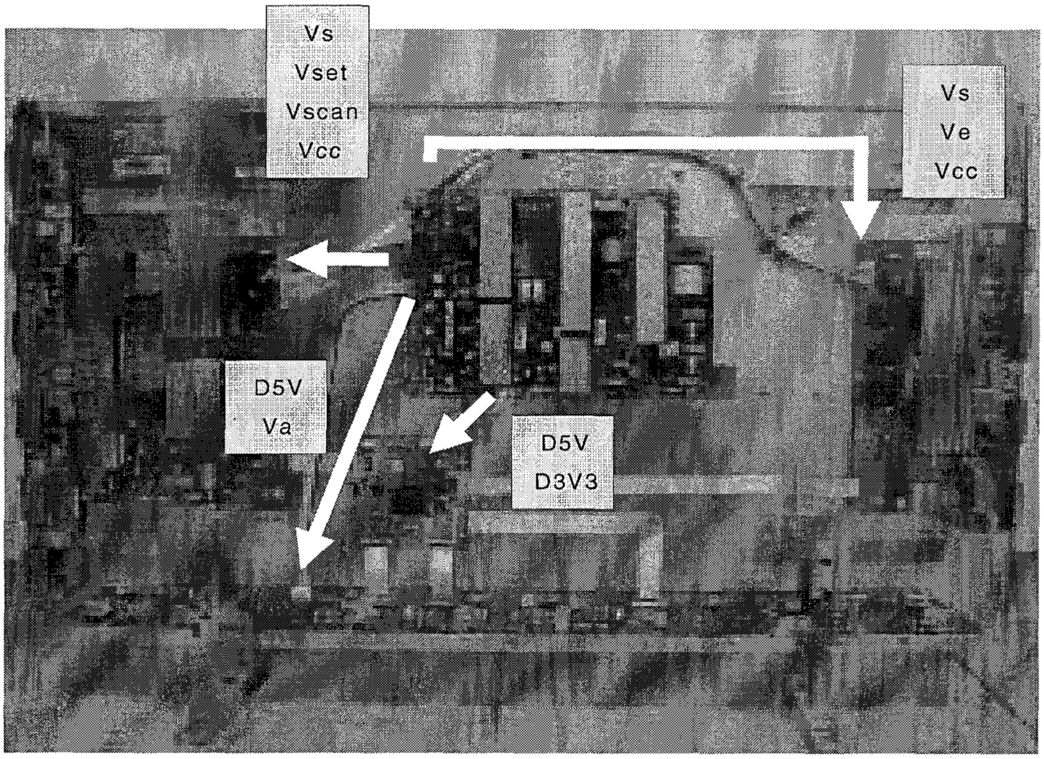
5.5V (5.5V) – F4004

Figure 8-8 Location of the test points for the supply voltages - X-main - 42" HD w1

8.1.5 Adjustment Power Supply Voltages 50" HD w1

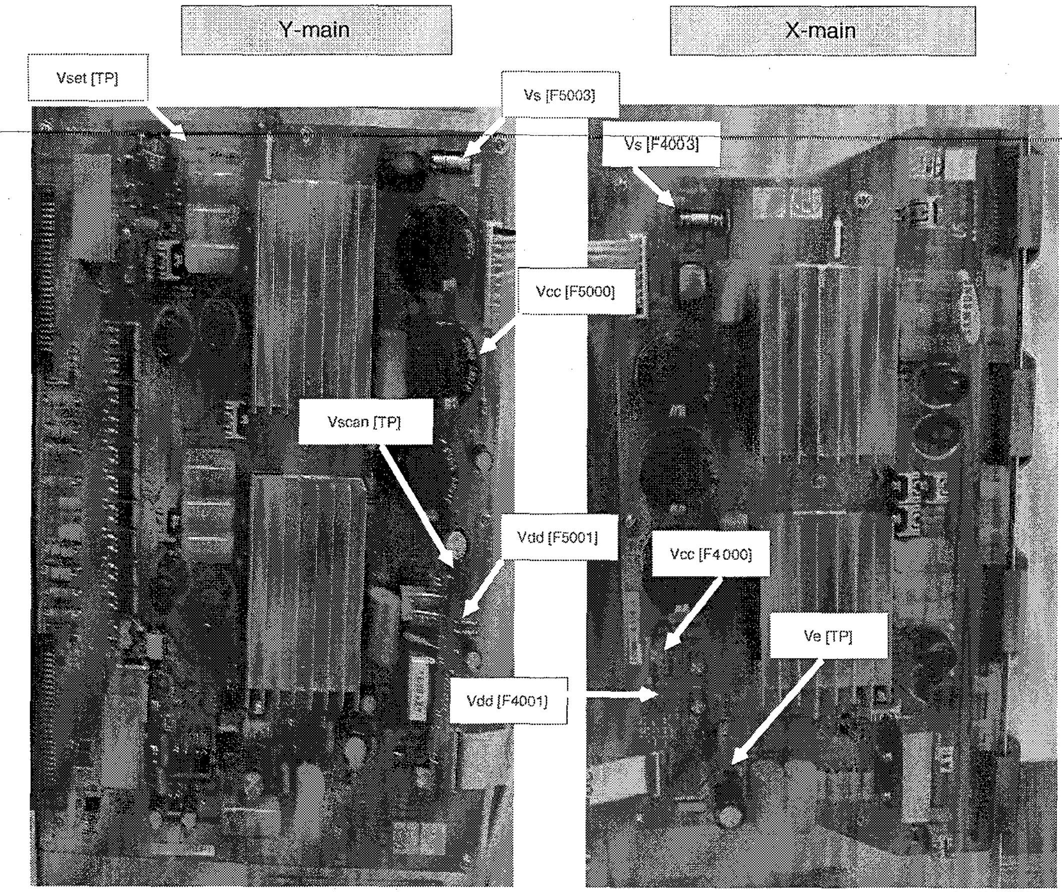
Table 8-3 Adjustment voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	VS	202 V ± 1 %	190 V ~ 210 V
2	VA	65 V ± 1.5 %	55 V ~ 75 V
3	VE	115 V ± 1.5 %	110 V ~ 130 V
4	VSET	190 V ± 1.5 %	170 V ~ 200 V
5	VSCAN	-190 V ± 1.5 %	-210 V ~ -180 V
6	VSB	5 V ± 5 %	Fixed
7	VG	15 V ± 5 %	Fixed
8	D5VL	5.2 V ± 5 %	Fixed
9	D3V3	3.3 V ± 5 %	Fixed
Check voltage label on the PDP for correct values.			


Vs
Vset
Vscan
Vcc
Vs
Ve
Vcc
D5V
Va
D5V
D3V3

G_16380_506.eps
160606

Figure 8-9 Location of the supply lines from the PSU to the boards - 50" HD w1


Y-main
X-main
Vset [TP]
Vs [F5003]
Vs [F4003]
Vcc [F5000]
Vscan [TP]
Vdd [F5001]
Vcc [F4000]
Ve [TP]
Vdd [F4001]

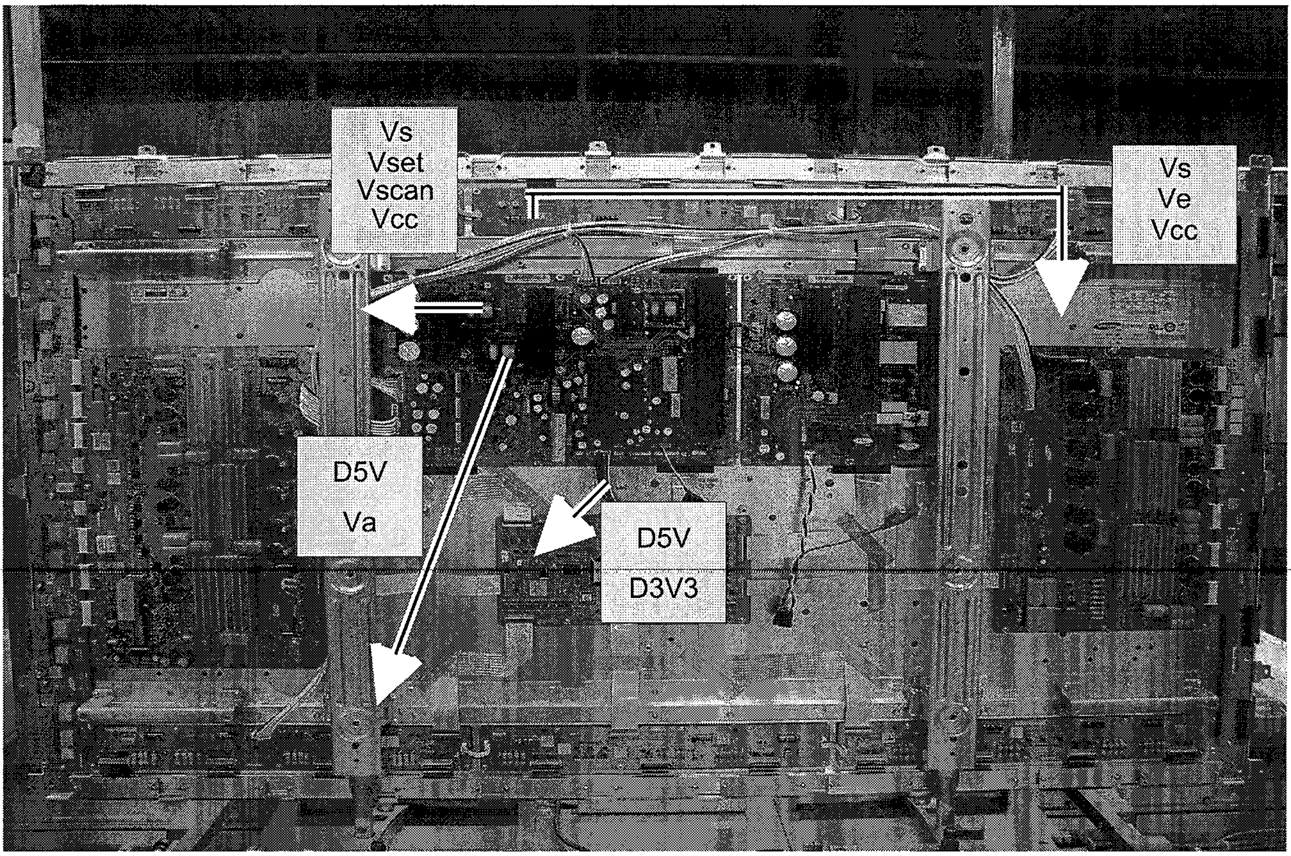
G_16380_507.eps
160606

Figure 8-10 Location of the test points for the supply voltages - 50" HD w1

8.1.6 Adjustment Power Supply Voltages 63" HD v4

Table 8-4 Adjustment voltage level overview (also refer to the sticker on the rear side of the panel)

No	Output voltage (V)	Voltage Setting (Normal Load)	Output Voltage Range
1	Vs	184 V ± 1 %	165 V ~ 190 V
2	Va	72 V ± 1.5 %	60 V ~ 85 V
3	Ve	88 V ± 1.5 %	80 V ~ 110 V
4	Vset	178 V ± 1.5 %	160 V ~ 200 V
5	Vscan	-160 V ± 1.5 %	-190 V ~ -155 V
6	Vsb	5 V ± 5 %	Fixed
7	Vg	15 V ± 5 %	Fixed
8	D5VL	5.3 V ± 5 %	Fixed
9	D3V3	3.4 V ± 5 %	Fixed
Check voltage label on the PDP for correct values.			



G_16380_055.eps
171006

Figure 8-11 Location of the supply lines from the PSU to the boards - 63" HD v4

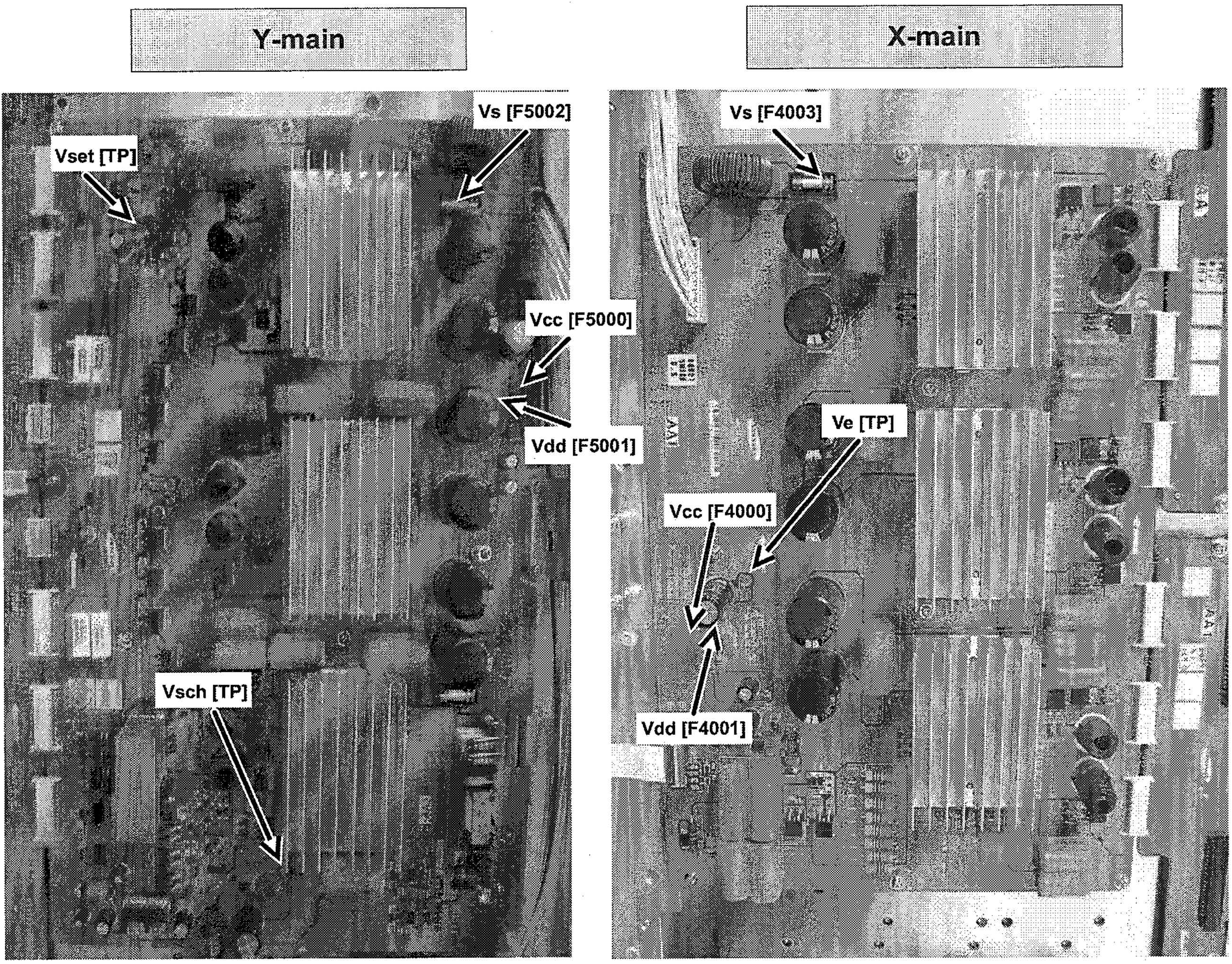
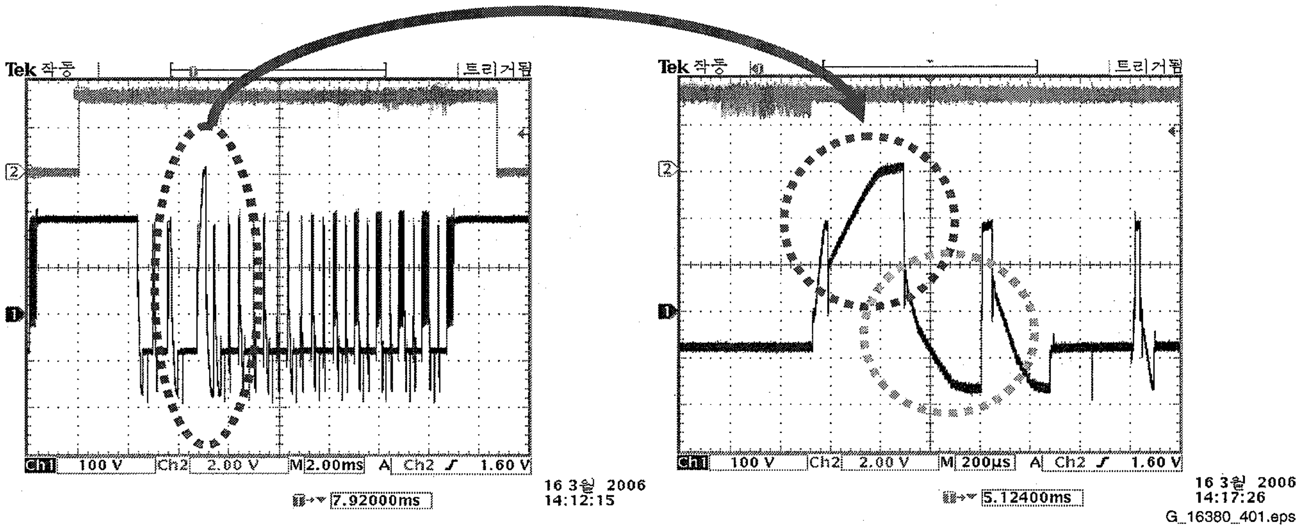

Y-main
X-main
Vset [TP]
Vs [F5002]
Vcc [F5000]
Vdd [F5001]
Vsch [TP]
Vs [F4003]
Ve [TP]
Vcc [F4000]
Vdd [F4001]
G_16380_057.eps
171006

Figure 8-12 Location of the test points for the supply voltages - 63" HD v4

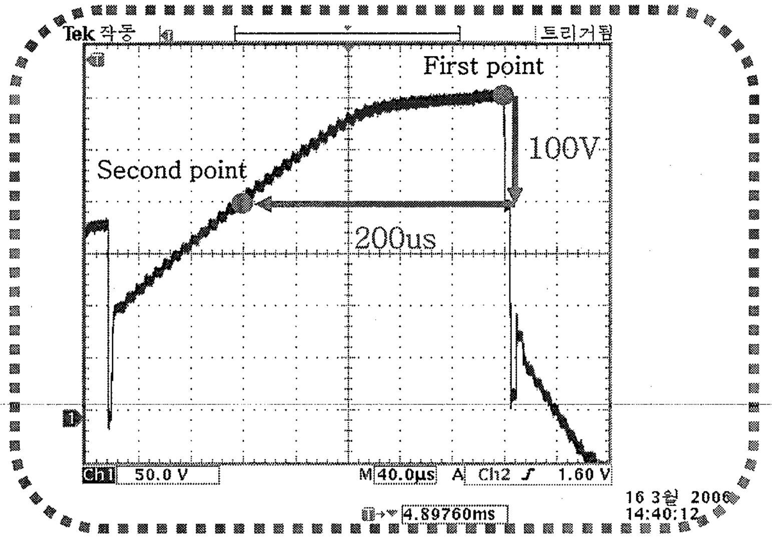
8.2 Waveform Alignments 42" SD v5

1. Set the pattern to Full White (put a jumper on pins 1 and 2 of CN2012 of the Logic Board).
2. Check the waveform using an Oscilloscope.
   - Triggering through V_TOGG of the LOGIC Board (see Figure "Logic PWB").
   - Connect the "OUT240" test point, located at the centre of the Y-buffer PWB, to the other channel, and then check the first Subfield waveform of one TV-Field.
   - Check the waveform by adjusting the Horizontal Division of the oscilloscope.
3. Adjust the waveform of the rising ramp with VR5000 (see Figure "Rising ramp waveform adjustment").
4. Adjust the waveform of the falling ramp with VR5001 (see Figure "Falling ramp waveform adjustment").



G_16380_401.eps
160606

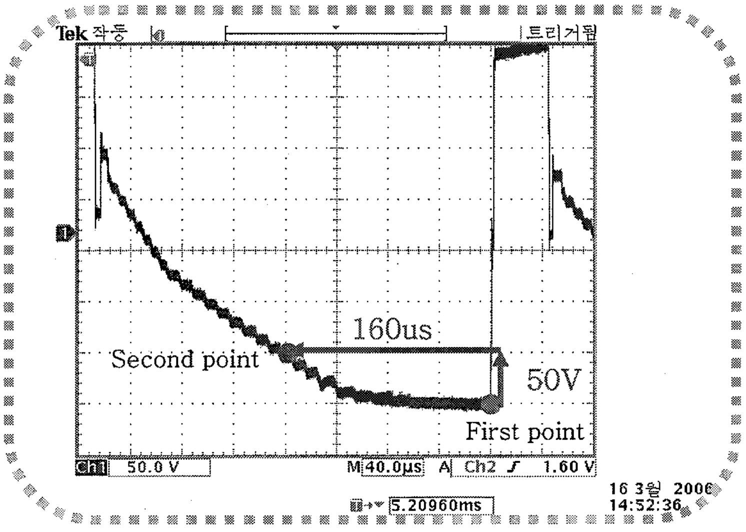
Figure 8-13 Waveform adjustment (Y-Board) - 42 SD v5



<Rising ramp>
The second point is located 100 V below and 200 usec before the first point.

G_16380_402.eps
160606

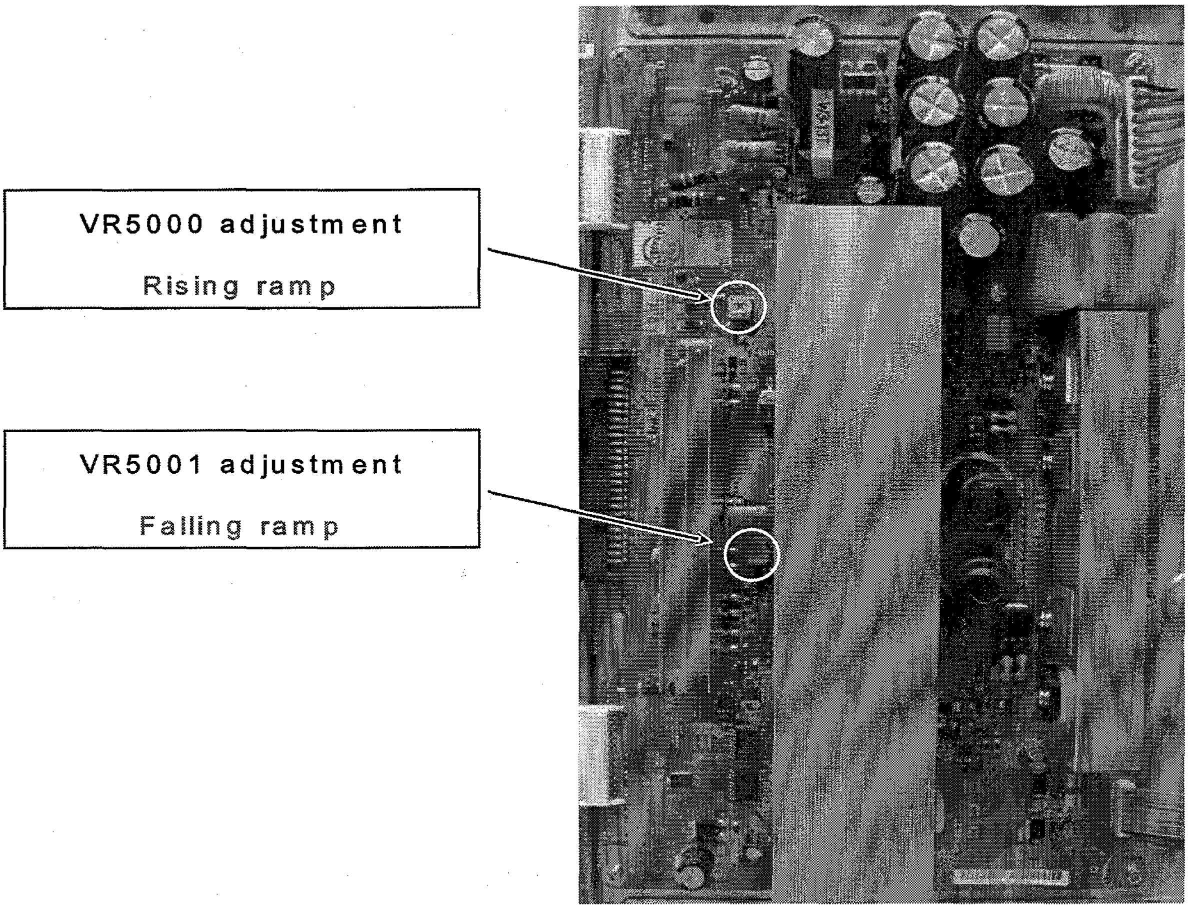
Figure 8-14 Rising ramp waveform (Y-Board) - 42 SD v5



<Falling ramp>
The second point is located 50 Volt above and 160 usec before the first point.

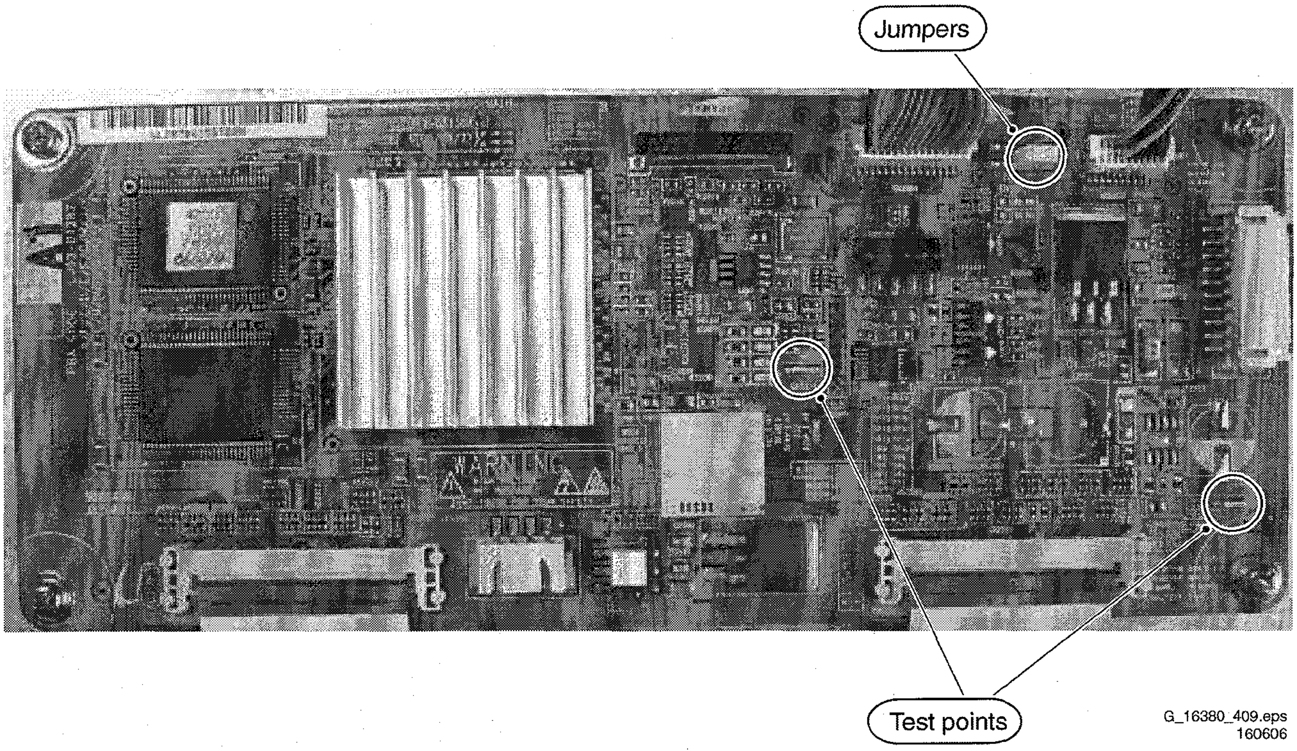
G_16380_403.eps
160606

Figure 8-15 Falling ramp flat time adjustment (Y-Board) - 42 SD v5


VR5000 adjustment
Rising ramp
VR5001 adjustment
Falling ramp

G_16380_404.eps
160606

Figure 8-16 Potentiometer locations - 42 SD v5

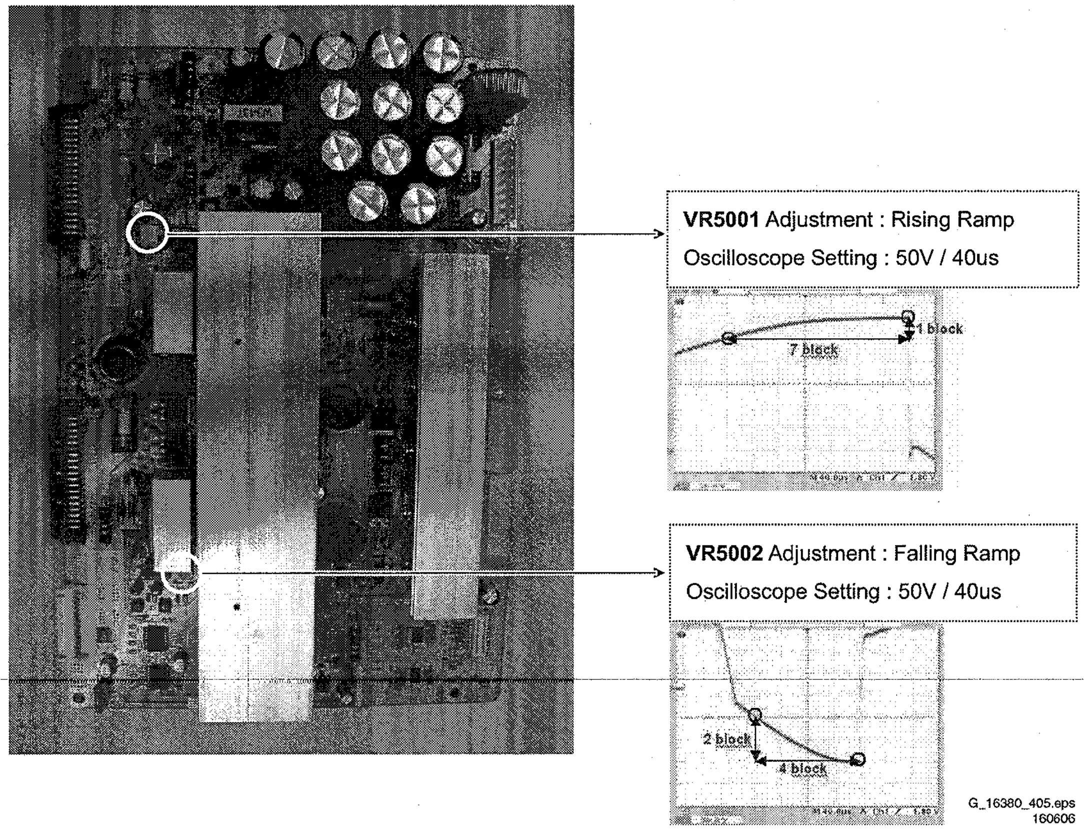

Jumpers
Test points

G_16380_409.eps
160606

Figure 8-17 Logic PWB - 42 SD v5

8.3 Waveform Alignments 42" HD w1

1. Set the pattern to Full White:
   - Place jumpers on:
     - J8902 of the PSU alarm board
     - J5003 and J5004 of the PSU
     - Pins 1 and 2 of CN2072 on the Logic Board
   - When the display starts showing a cycle of different patterns, push button SW2001 for at least one second. Now the display shows a continuous full white pattern. To restart the cycle of different patterns, push the button once more and wait for a few seconds.
2. Check the waveform using an Oscilloscope.
   - Triggering through V_TOGG of the LOGIC Board (see Figure "Logic PWB").
   - Connect the "OUT240" test point, located at the centre of the Y-buffer PWB, to the other channel, and then check the first Subfield waveform of one TV-Field.
   - Check the waveform by adjusting the Horizontal Division of the oscilloscope.
   - Check the waveform by adjusting the Horizontal Division of the oscilloscope.
   - Check the Reset waveform when the V_TOGG level is changed.
3. Adjust the waveform of the rising ramp with VR5001 (see Figure "Rising ramp waveform adjustment").
4. Adjust the waveform of the falling ramp with VR5002 (see Figure "Falling ramp waveform adjustment").



VR5001 Adjustment : Rising Ramp

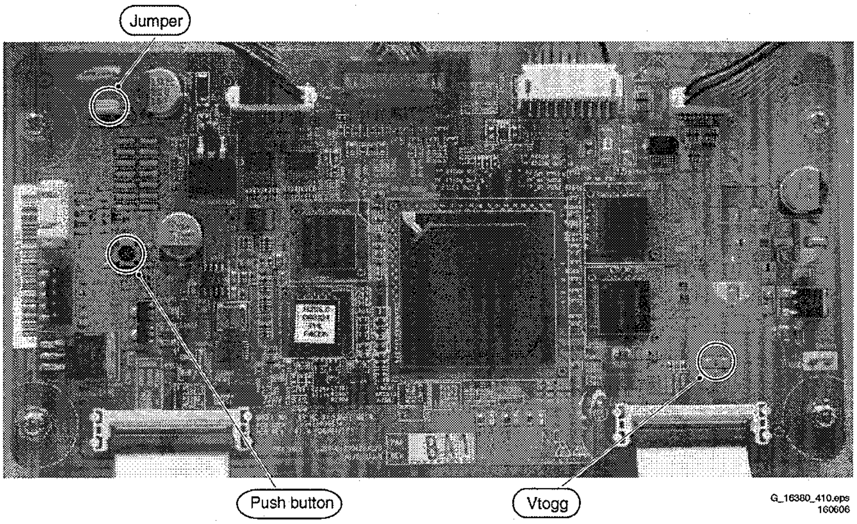
Oscilloscope Setting : 50V / 40us

VR5002 Adjustment : Falling Ramp

Oscilloscope Setting : 50V / 40us

G_16380_405.eps
160606

Figure 8-18 Adjusting procedure - 42" HD w1



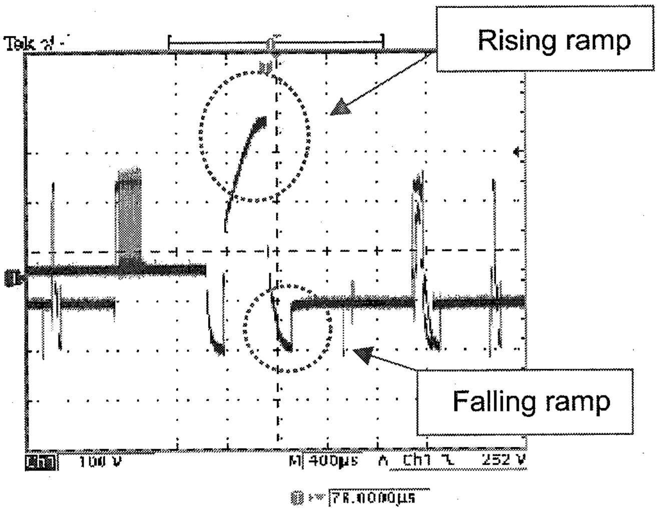
G_16380_410.eps
160606

Figure 8-19 Logic PWB - 42 HD w1

8.4 Waveform Alignments 50" HD w1

1. Set the pattern to Full White:
   - Place jumpers on:
     - J8902 of the PSU alarm board
     - J5003 and J5004 of the PSU
     - Pin 1 and 2 of CN2072 on the Logic Board
   - When the display starts showing a cycle of different patterns, push button SW2001 for at least one second. Now the display shows a continuous full white pattern. To restart the cycle of different patterns, push the button once more and wait for a few seconds.
2. Check the waveform using an Oscilloscope.
   - Triggering through V_TOGG of the LOGIC Board (see Figure "Logic PWB").
   - Connect the "OUT240" test point, located at the centre of the Y-buffer PWB, to the other channel, and then check the first Subfield waveform of one TV-Field.
   - Check the waveform by adjusting the Horizontal Division of the oscilloscope.
   - Check the waveform by adjusting the Horizontal Division of the oscilloscope.
   - Check the Reset waveform when the V_TOGG level is changed.
3. Adjust the waveform of the rising ramp with VR5001 (see Figure "Rising ramp waveform adjustment").
4. Adjust the waveform of the falling ramp with VR5002 (see Figure "Falling ramp waveform adjustment").

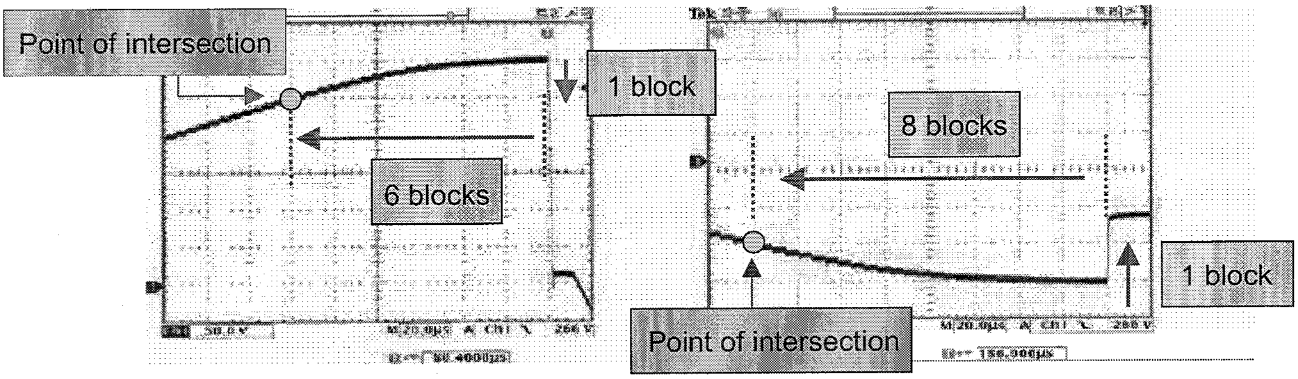
Special notice: It is very important, that you execute this adjustment on the 1st Sub-Field (SF) of the 1st Frame of the Reset waveform and then move to the 3rd Sub-field for adjusting.



< Main Reset Waveform>

Adjust VR5000 to set the time of Yrr (Main Reset Rising Ramp) like the below picture.
Oscilloscope Setting : 50V / 20us

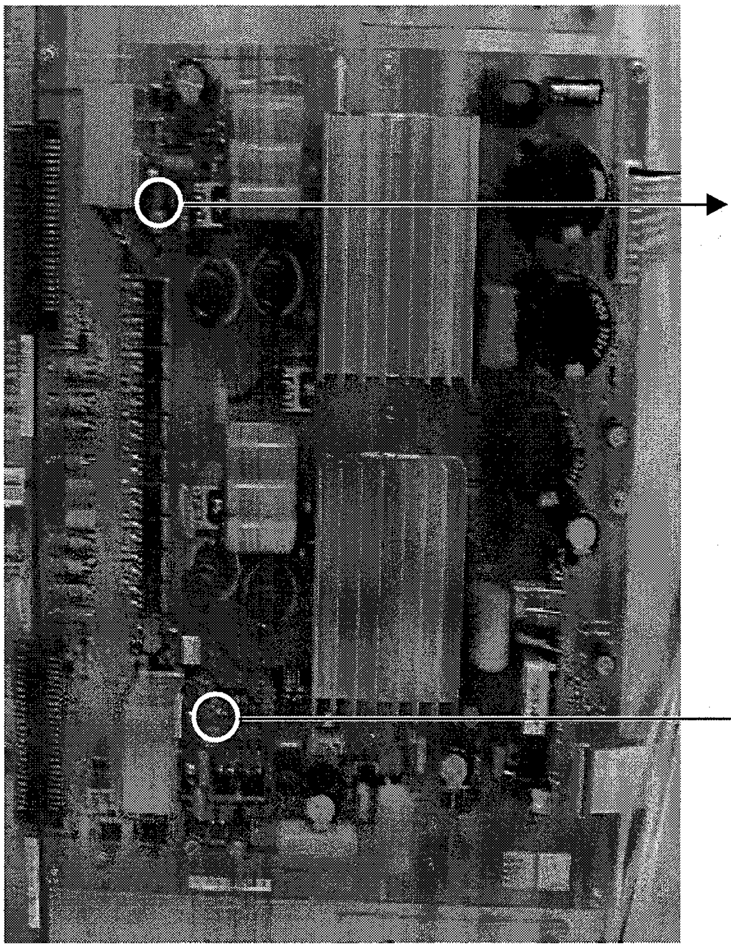
Adjust VR5001 to set the time of Yfr (Main Reset Falling Ramp) like the below picture.
Oscilloscope Setting : 50V / 20us



<Rising Ramp> **<Falling Ramp>**

G_16380_406.eps
160606

Figure 8-20 TCP ramp waveform inclination adjustment (Y-Board)



VR5000 Adjustment :

Adjust VR5000 to set the time of Yrr (Main Reset Rising Ramp) like the picture of front page.

Oscilloscope Setting : 50V / 20us

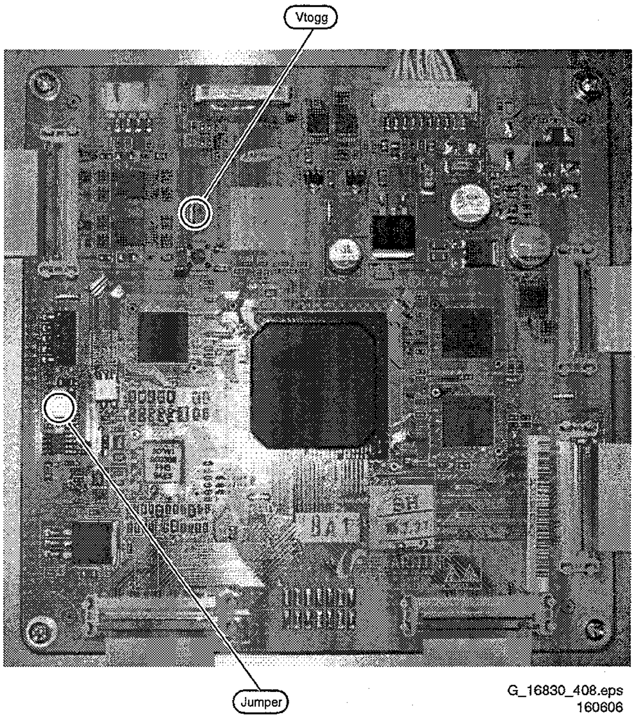
VR5001 Adjustment :

Adjust VR5001 to set the time of Yfr (Main Reset Falling Ramp) like the picture of front page.

Oscilloscope Setting : 50V / 20us

G_16380_407.eps
160606

Figure 8-21 Potentiometer locations (Y-Board) - 50 HD w1



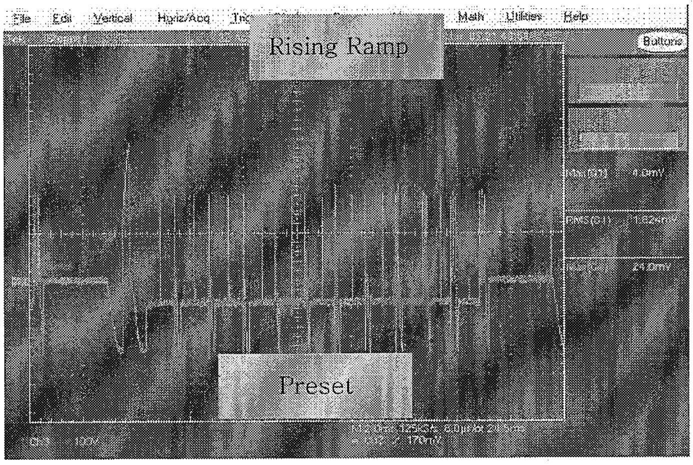
G_16830_408.eps
160606

Figure 8-22 Logic Main board - 50 HD w1

8.5 Waveform Alignments 63" HD v4

1. Set the pattern to Full White:
   - Place a jumper on CN2012 on the Logic Board and switch the display "ON".
2. Check the waveform using an Oscilloscope.
   - Triggering through V_TOGG of the LOGIC Board (see Figure "Logic PWB").
   - Connect the "OUT240" test point, located at the centre of the Y-buffer PWB, to the other channel, and then check the first Subfield operating waveform of one TV-Field.
   - Check the waveform by adjusting the Horizontal Division of the oscilloscope.
   - Check the Reset waveform when the V_TOGG level is changed.
3. Adjust the intersection point of the rising ramp with VR5000 (see Figure "Rising ramp waveform adjustment").
4. Adjust the intersection point of the falling ramp with VR5001 (see Figure "Falling ramp waveform adjustment").

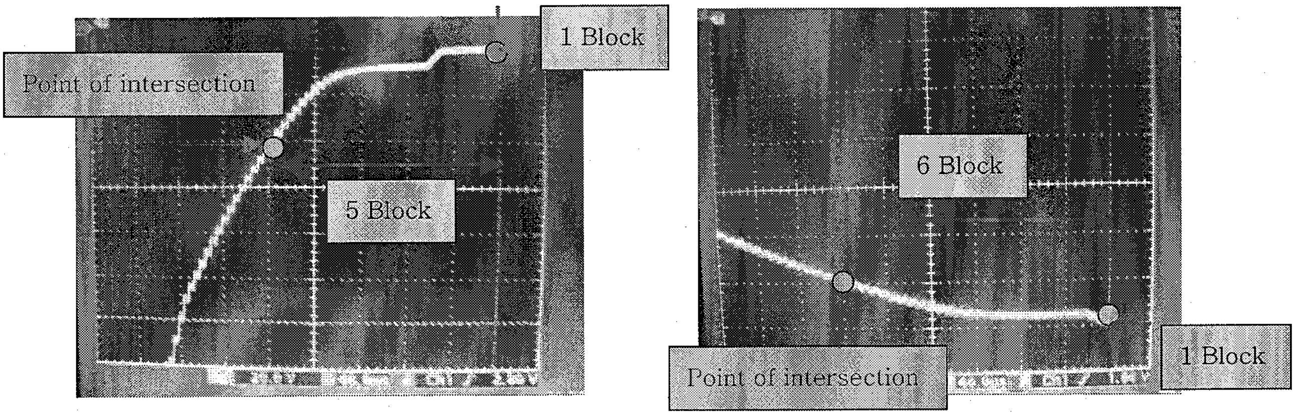
W1 Ramp Waveform Inclination Adjustment (Y-Board)



< Main Reset Waveform>

Adjust VR5000 to set the time of Yrr (Main Reset Rising Ramp) like the below picture.
Oscilloscope Setting : 20V / 40us

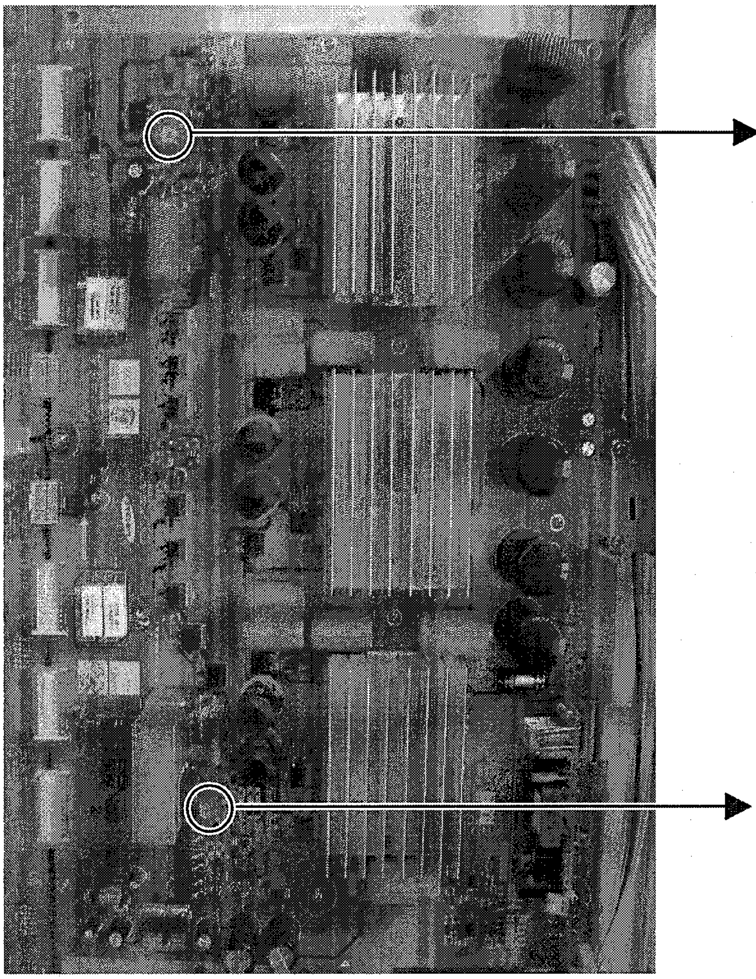
Adjust VR5001 to set the time of Yfr (Preset) like the below picture.
Oscilloscope Setting : 20V / 40us



<Rising Ramp> **<Preset>**

G_16380_061.eps
181006

Figure 8-23 TCP ramp waveform inclination adjustment (Y-Board)



VR5000 Adjustment :

Adjust VR5000 to set the time of Yrr (Main Reset Rising Ramp) like the picture of the previous page.

Oscilloscope Setting : 20V / 40us

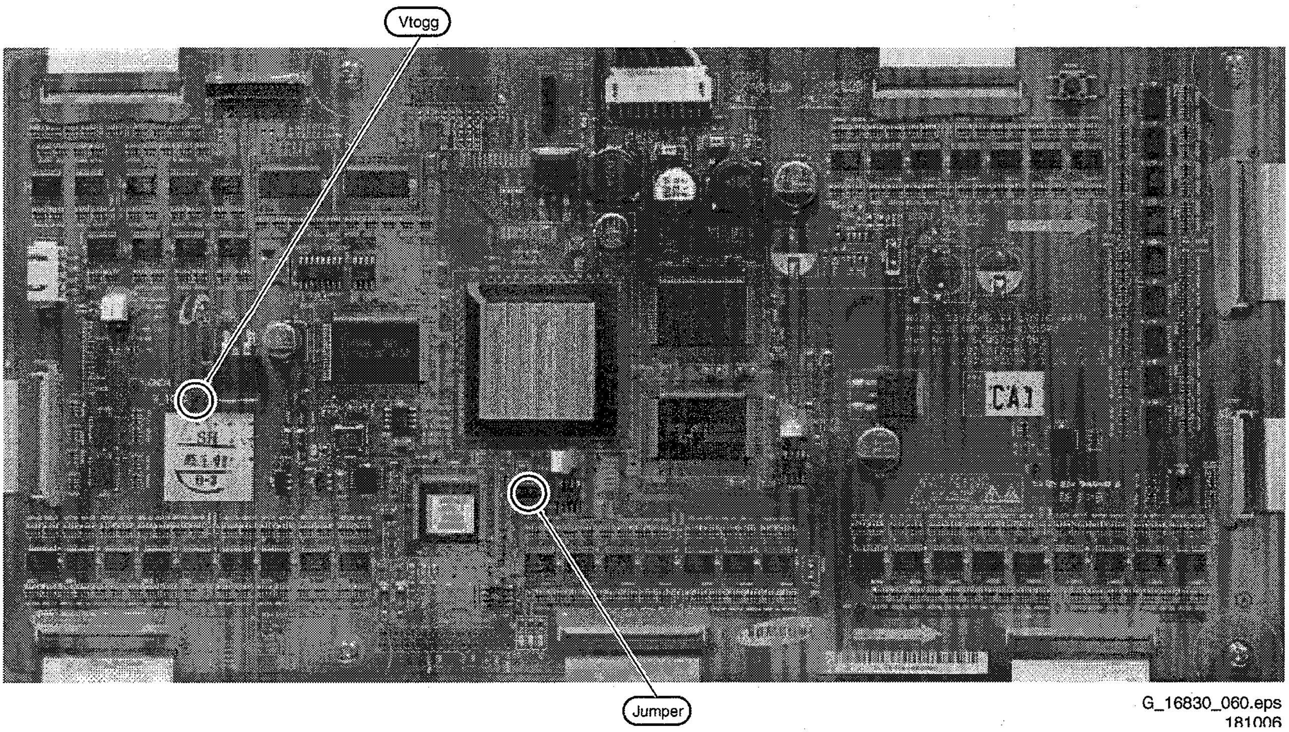
VR5001 Adjustment :

Adjust VR5001 to set the time of Yfr (Preset) like the picture of the previous page.

Oscilloscope Setting : 20V /40us

G_16380_062.eps
181006

Figure 8-24 Potentiometer locations (Y-Board) - 50 HD w1



G_16830_060.eps
181006

Figure 8-25 Logic Main board - 63" HD v4

9. Circuit Descriptions, Abbreviation List, and IC Data Sheets

Index of this chapter:

9.1 Main function of Each Assembly
9.2 Abbreviation List
9.3 IC Data Sheets

9.1 Main function of Each Assembly

9.1.1 X Main Board

The X Main board generates a drive signal by switching the FET in synchronization with logic main board timing, and supplies the X electrode of the panel with the drive signal through the connector.

1. Maintain voltage waveforms (including ERC).
2. Generate X rising ramp signal.
3. Maintain Ve bias between Scan intervals.

9.1.2 Y Main Board

The Y Main board generates a drive signal by switching the FET in synchronization with the logic Main Board timing and sequential supplies the Y electrode of the panel with the drive signal through the scan driver IC on the Y-buffer board. This board connected to the panel's Y terminal has the following main functions.

1. Maintain voltage waveforms (including ERC).
2. Generate Y-rising Falling Ramp.
3. Maintain V scan bias.

9.1.3 Logic Main Board

The Logic Main board generates and outputs the address drive output signal and the X,Y drive signal by processing the video signals. This Board buffers the address drive output signal and feeds it to the address drive IC (COF module, video signal- X Y drive signal generation, frame memory circuit / address data rearrangement).

9.1.4 Logic Buffer (E, F)

The Logic Buffer transmits data signal and control signal.

9.1.5 Y Buffer Board (Upper, Lower)

The Y Buffer board consisting of the upper and lower boards supplies the Y-terminal with scan waveforms. The board comprises eight scan driver ICs (ST microelectronics STV 7617: 64 or 65 output pins), but four ICs for the SD class.

9.1.6 AC Noise Filter

The AC Noise filter has function for removing noise (low frequency) and blocking surge. It affects safety standards (EMC, EMI).

9.1.7 TCP (Tape Carrier Package)

The TCP applies the Va pulse to the address electrode and constitutes address discharge by the potential difference between the Va pulse and the pulse applied to the Y electrode. The TCP comprise four data driver ICs (STV7610A: 96 pins output pins). Seven TCPs are required for signal scan.

9.2 Abbreviation List

AC	Alternating Current
COF	Circuit On Foil
DC	Direct Current
ERC	Energy Recovery Circuit
ESD	Electro Static Discharge
FET	Field Effect Transistor
FFC	Flat Foil Cable
FPC	Flexible Printed Circuit
FTV	Flat TeleVision
HD	High Definition
I/O	Input/Output
IC	Integrated Circuit
LB	Logic Buffer
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signalling
PCB	Printed Circuit Board (same as PWB)
PDP	Plasma Display Panel
PSU	Power Supply Unit
PWB	Printed Wiring Board (same as PCB)
RGB	Red, Green, Blue colour space
SD	Standard Definition
SDI	Samsung Display Industry (supplier)
SMPS	Switched Mode Power Supply
SSB	Small Signal Board
SF	Sub Field
TCP	Tape Carrier Package
VR	Variable Resistor
Vsc	Scan Voltage
YBL	Y Buffer Lower board
YBU	Y Buffer Upper board
YM	Y Main board

9.3 IC Data Sheets

Not applicable.

10. Spare Parts List

Notes;

- Determine the SDI part / model number of the PDP.
- Find the SDI part number on the actual board to be replaced.
  SDI part numbers begin with "LJ92", except for the SMPS the part number begins with "LJ44".
- Find the SDI board part number in the spare parts overview.
- Find the SDI part number in this overview that matches the part number that is actually on the original board.
- Cross the SDI board part number to the Philips part number.
- Order the Philips part number.

- **Note:** The appearance of a leaded and lead-free board can be different; the colour of the PWB and also the layout of the components are sometimes different.

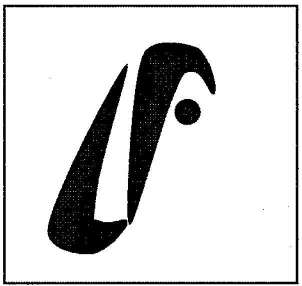


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Figure 10-1 Lead-free logo SDI

Table 10-1 Spare parts overview

PDP type	**42 SD v5**		**42 HD w1**		**50 HD w1**		**63 HD v4**	
PDP 12 NC	**9322 233 14682**		**9322 240 08682**		**9322 240 25682**		**9322 246 18682**	
PDP model type and version	S42SD-YD09	PP42SD-019A	S42AX-YD02	PP42AX-009A	S50HW-YD01	PP50HW-010A	S63HW-YD05	PP63HW-005A
BOARDS	**SDI part #**	**12NC**	**SDI part #**	**12NC**	**SDI part #**	**12NC**	**SDI part #**	**12NC**
Logic-Buffer (E)	LJ92-01322B	9965 000 37577	LJ92-01343A	9965 000 36813	LJ92-01372A	9965 000 36826	LJ92-01193A	9965 000 42586
Logic-Buffer (F)	LJ92-01323B	9965 000 37608	LJ92-01342A	9965 000 36814	LJ92-01373A	9965 000 36827	LJ92-01194A	9965 000 42587
Logic-Buffer (G)	-	-	-	-	LJ92-01374A	9965 000 36828-	LJ92-01195A	9965 000 42588-
Y-Buffer	LJ92-01339A	9965 000 36812	LJ92-01344A	9965 000 36819	-	-	-	-
Y-Buffer (up)	-	-	-	-	LJ92-01276C	9965 000 36824	LJ92-01437A	9965 000 42589
Y-Buffer (down)	-	-	-	-	LJ92-01277C	9965 000 36825	LJ92-01438A	9965 000 42590
Logic-Board	LJ92-01287C	9965 000 37576	LJ92-01370B	9965 000 36815	LJ92-01371B	9965 000 36820	LJ92-01289C	9965 000 36820
X-Main Board	LJ92-01340A	9965 000 36810	LJ92-01345A	9965 000 36817	LJ92-01388A	9965 000 36822	LJ92-01385A	9965 000 42594
Y-Main Board	LJ92-01341A	9965 000 36811	LJ92-01346A	9965 000 36818	LJ92-01391A	9965 000 36823	LJ92-01386A	9965 000 42595
SMPS (PSU)	LJ44-00101C	9965 000 33880	LJ44-00117A	9965 000 36816	LJ44-00118A	9965 000 36821	LJ44-00123A	9965 000 42596
SMPS (Sub PSU)	-	-	-	-	-	-	LJ44-00124A	9965 000 42597
X-Buffer (up)	-	-	-	-	-	-	LJ92-01375A	9965 000 42591
X-Buffer (down)	-	-	-	-	-	-	LJ92-01376A	9965 000 42592
CABLES + CONNECTORS	**SDI part #**	**12NC**	**SDI part #**	**12NC**	**SDI part #**	**12NC**	**SDI part #**	**12NC**
Cable-flat Logic + Y-Main	LJ39-00164A	9965 000 37609	LJ39-00265A	9965 000 37612	3809-001789	9965 000 37614	3809-001546	996500042799
Cable-flat Logic + X-Main	LJ39-00252A	9965 000 37610	LJ39-00264A	9965 000 37613	3809-001788	9965 000 37615	3809-001695	996500042800
Cable-flat Logic + Logic Buf (E)	3809-001791	9965 000 37611	3809-001629	9965 000 37617	3809-001771	9965 000 37618	-	-
Cable-flat Logic + Logic Buf (F)	3809-001791	9965 000 37611	3809-001629	9965 000 37617	3809-001771	9965 000 37618	-	-
Cable-flat Logic + Logic Buf (G)	-	-	-	-	3809-001790	9965 000 37616	-	-
Cable-flat Logic + Logic Buf (E) upper	-	-	-	-	-	-	3809-001743	996500042801
Cable-flat Logic + Logic Buf (F) upper	-	-	-	-	-	-	3809-001742	996500042802
Cable-flat Logic + Logic Buf (G) upper	-	-	-	-	-	-	3809-001745	996500042803
Cable-flat Logic + Logic Buf (E) lower	-	-	-	-	-	-	3809-001744	996500042804
Cable-flat Logic + Logic Buf (F) lower	-	-	-	-	-	-	3809-001741	996500042805
Cable-flat Logic + Logic Buf (G) lower	-	-	-	-	-	-	3809-001768	996500042806
Connector Logic Buf (E)+Logic Buf (F)	LJ39-00202A	9965 000 37619	LJ39-00259A	9965 000 37623	LJ39-00257A	9965 000 37627	LJ39-00215A	996500042807
Connector Logic Buf (F)+Logic Buf (G)	-	-	-	-	LJ39-00257A	9965 000 37627	LJ39-00215A	996500042807
Connector SMPS + Logic Buf (E)	LJ39-00256A	9965 000 37620	LJ39-00241A	9965 000 37624	LJ39-00266A	9965 000 37628	-	-
Connector SMPS + Logic Buf (E) upper	-	-	-	-	-	-	LJ39-00234A	996500042808
Connector SMPS + Logic Buf (E) lower	-	-	-	-	-	-	LJ39-00184A	996500042809
Connector SMPS + Logic Main	LJ39-00209A	9965 000 37621	LJ39-00155A	9965 000 37625	LJ39-00266A	9965 000 37628	LJ39-00293A	996500042810
Connector SMPS + Y-Main	LJ39-00263A	9965 000 37626	LJ39-00263A	9965 000 37626	LJ39-00221A	9965 000 37629	LJ39-00239A	996500042811
Connector SMPS + X-Main	LJ39-00262A	9965 000 37622	LJ39-00262A	9965 000 37622	LJ39-00220A	9965 000 37630	LJ39-00185A	996500042812
CTN / Chassis	**CTN**	**Chassis**	**CTN**	**Chassis**	**CTN**	**Chassis**	**CTN**	**Chassis**
Sets/Chassis in which this PDP type is used (this list is for indicative purposes only, we do not pretend it is complete)	42PF5521D/10	LC4.41E AB	42PF9431D/37	BJ2.5U PA	50PF9631D/37	BJ2.4U PA	63PF9631D/37	BJ3.0U PA
	42PF5521D/12	LC4.41E AB	42PF9631D/37	BJ2.4U PA	50PF9731D/37	BJ2.4U PA	-	-

11. Revision List

Manual xxxx xxx xxxx.0

- First release.

Manual xxxx xxx xxxx.1

- Name changed from “SDI PDP Repair Manual” to “SDI PDP 2K6”.
- Model 63” HD v4 added.